TECHNICAL BULLETIN

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HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 15 January 1979

SUPPLEMENTARY OPERATING INSTRUCTIONS

TEST SET, INTEGRATED CIRCUIT CARD

TESTERS AN/USM-371 AND AN/USM-371A

PRINTED CIRCUIT CARD TEST PROGRAMS FOR SYNCHRONIZER, ELECTRICAL SN-394(V)/G (CARDS A-1 THROUGH A-6) AND FOR ROUTING SET, TELETYPEWRITER AN/FGC-73(V) (CARDS 200000G1 THROUGH 200160G1)

REPORTING OF ERRORS

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1. Purpose. This technical bulletin provides supplementary instructions in the form of test programs and associated data for troubleshooting printed circuit cards A-1 through A-6 of Synchronizer, Electrical SN-394(V)/G and printed circuit cards 200000G1 through 200160G1 of Routing Set, Teletypewriter AN/FGC-73(V), using Test Set, Integrated Circuit Card Tester AN/USM-371 and AN/USM-371A.

NOTE:

Nomenclature	Model Number
AN/USM-371	Model ICT-102
AN/USM-371A	Model ICT-103

2. Test Procedures. Refer to the general instructions to become familiar with the basic data required for troubleshooting the faulty printed circuit card. Locate the schematic diagram and test data that pertain to the faulty card. Operate the test set to isolate the fault as described in the operating procedures.

Dynatronics Products

PC CARD TEST PROGRAMS
for the
MODEL ICT - 102 and ICT - 103
PRINTED CIRCUIT CARD TESTER

INTEGRATED CIRCUIT CARD TEST SET
AN/USM-371 and AN/USM-371A
used for
AUTODIN PC CARDS
200000G1 through PL-1119/G A-6 (SN-394)

PROGRAM MANUAL

GENERAL DYNAMICS
Electro Dynamic Division

LIST OF EFFECTIVE PAGES

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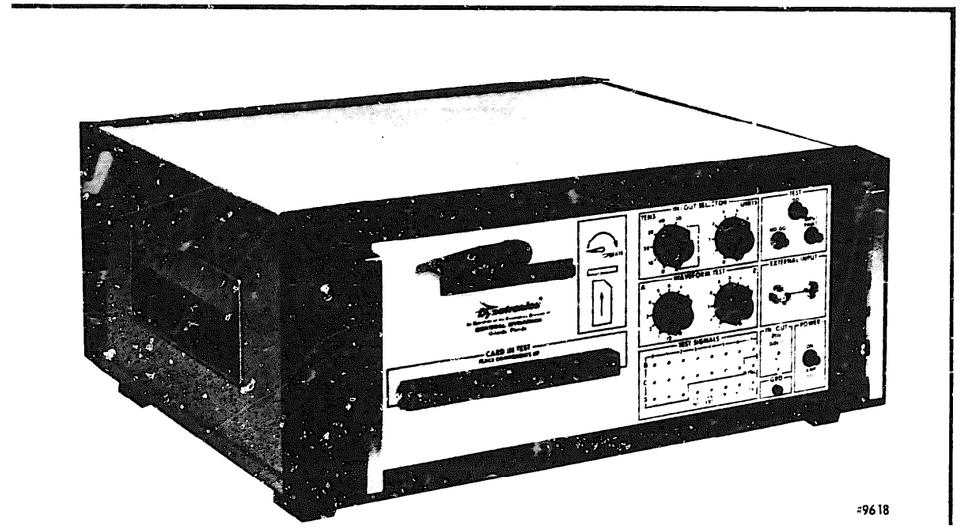
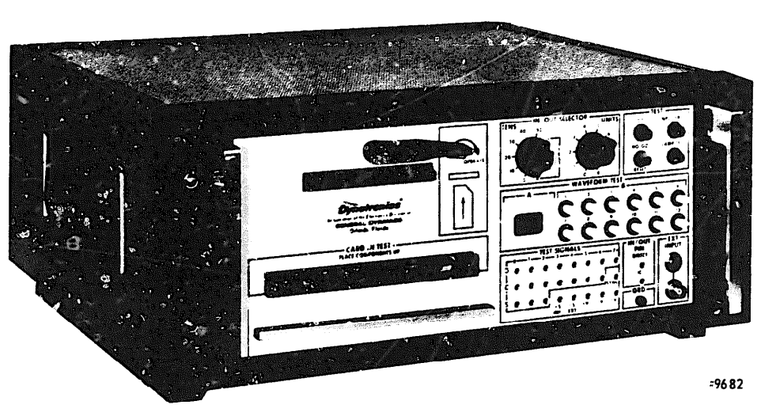
Dynatronics Printed Circuit Card tester models ICT-102 and ET-103 provide the capability for dynamically testing virtually any logic family on a visual basis. Punched Hollerith cards contain individual programs which eliminate elaborate test hook-ups normally found during testing operations. No external test equipment is necessary because complete dynamic tests are performed by the Card Tester each time an individual program card is inserted into the card reader. All conditions (signal generation, power distribution, grounding, loading, test rates, etc.) are controlled by the program card and all circuits are fully tested by following a simple set of instructions and observing the GO/NO-GO and FAULT indicator lamps on the front panel. These instructions are provided in the following paragraphs.

Differences in the two models (ICT-102 and ICT-103) are illustrated in figure 1, Basically the card testers function alike with the main differences being in operator switch setting procedures. The model ICT-102 Card Tester uses rotary switches for selecting circuit under test output signal GO/NO-GO test parameters whereas the model ICT-103 Card Tester features pushbuttons in place of the rotary switches. Individual card test documentation provided in this manual can be used for either model Card Tester.



MODEL ICT-102 CARD TESTER



MODEL ICT-103 CARD TESTER

Figure 1. Printed Circuit Card Testers (100 Series)

CARD TESTER SCHEMATIC OR LOGIC DIAGRAM MARKINGS

Each schematic or logic diagram associated with individual programmed cards are marked such that pertinent information related to signal routing, power distribution, and other test requirements are readily available to the test technician. Markings and symbols normally found on schematic or logic diagrams are listed below:

a. Parenthesis - Used to enclose test information such as pin numbers and test signals generated by the card tester and routed to the card-under-test via the card reader, i.e., (4) indicates that this pin connects to the card tester CARD IN TEST connector, pin 4; (+C0) indicates that test signal +CO is connected to the card-under-test via the card reader.

b. Symbol (H) - Placed adjacent to schematic wiring which remain at a high logic level throughout the test. A high logic level is defined as the upper level of the signal voltage levels.

c. Symbol (L) - Placed adjacent to schematic wiring which remain at a low logic level throughout the test. A low logic level is defined as the lower level of the signal voltage levels.

Note

All points not labeled (H) or (L)
are dynamic i.e., are switching
during the test.

d. -/-/-/-/-/-/-/-/-/-/- - This symbol indicates input or output lines which are not tested by the card tester test program. On cards which arc tested by two programs, the symbol indicates that the input or output line is not tested by either program.

e. (GRD) Symbol - Indicates that DC power ground from the card tester is applied to the card-under-test at this point.

f. (+Vcc) Symbol - Independent +5 20.5 volt power supply internal to the card tester used for supplying +Vcc to the card-under-test via the card test program. This pow& supply, +5 EXT, is adjusted from the rear panel of the card tester.

g. -+V, +V, -V Symbols - These symbols indicate which of the three programmable power supplies are connected to the card-under-test. The output voltage values for the programmable power supplies are located on the waveform sheet in the TEST PARAMETERS table.

h. (NC) Symbol - Indicates that there is no connection made between the referenced point on the card-under-test and the card tester.

These markings are located on the schematic drawings where applicable and are defined in the TEST LEGEND contained on each schematic. Definitions for the above markings apply to both the ICT-102 and ICT-103 Card Testers.

CARD TESTER WAVEFORM MARKINGS

Several symbols are used on the waveform charts to indicate special procedures required while testing a particular printed circuit card. These symbols and/or special instructions are located in the notes at the bottom of each waveform chart. Before proceeding with any test it is required that the notes be read and special instructions be carried out. For example, the notes may indicate that the Card Tester +5 volt external power supply be adjusted to +4.5 volts prior to testing the printed circuit card in question. In this case the printed circuit card could be damaged if the power supply had been adjusted to +5.5 volts for the preceeding test. Typical notes and symbols are described below:

a. Asterisk * Symbol - This symbol when placed adjacent to a pin number (either input or output pin) on the waveform chart indicates that the signal on that pin is inverted with respect to the waveform shown. Typically these symbols are located in the INPUT PINS and OUTPUT PINS columns of the waveform chart.

b. # Symbol - Indicates that no further edges are present in the output signal under test and the output is tested according to the steps for the model of Card Tester in use.

c. Encircled Output Fins - Encircled output pins are the more significant outputs that when tested check the majority of the circuits on the card-under-test. These output pins should be tested first to determine the general status of the card being tested. For example, when testing a multiple stage shift register with individual stages brought out on pins, the last stage of the shift register would be encircled and tested before the individual stages were tested. In this manner it is determined that the card is functionally operational after checking a single output pin.

MODEL ICT-102 OPERATING PROCEDURES

Following is the step-by-step procedure for performing dynamic test analysis on printed circuit cards programmed for the model ICT 102 Card Tester. These instructions pertain co all printed circuit cards: specific instructions peculiar to individual printed circuit cards undergoing tests are listed as notes on the appropriate waveform sheet. Waveform sheets for individual printed circuit cards are contained in this volume. Before proceeding with any test, the operator must read the notes contained on the waveform sheet and follow any specific instructions first. In addition the necessary card adapters, card extender cables, and programmable load boards should be inserted in the Card Tester to accommodate the card to be tested. The steps listed below provide the necessary information for successful diagnostic testing of all printed circuit cards programmed for testing with the ICT-102.

a. Refer to the appropriate card under test schematic or logic diagram and corresponding waveform sheet. On the waveform sheet, locate the notes and follow the instructions pertinent to the operator. Typically, the notes are located along the bottom edge of the waveform sheet.

b. Insert the PC card adapter and/or extender cable (if required) into the CARD IN TEST connector on the front panel of the Card Tester.

C. Insert the printed circuit card to be tested into the card adapter with the component side facing up.

d. Locate the corresponding card under test program card and insert it into the card reader slot as depicted on the front panel of the Card Tester. Push the programcard into the card reader slot until there is a noticeable resistance felt against the test card. Move the card reader handle clockwise until it is in the full closed position.

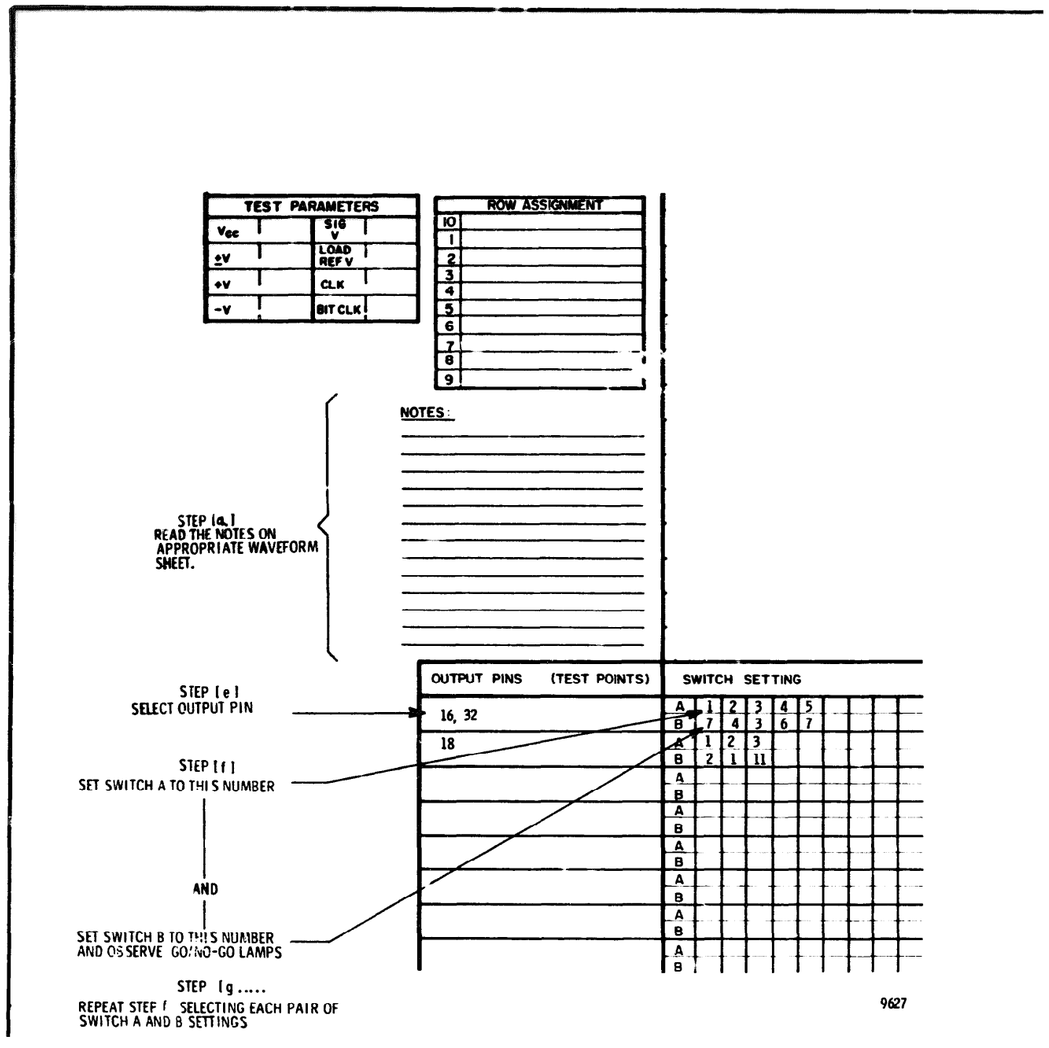


Figure 2. Model ICT-102 Waveform Sheet Example

Note

When initially energized, the Card Tester INPUT FAULT indicator is illuminated. Resetting the Card Tester should clear the INPUT FAULT indicator. If the INPUT FAULT indicator is not extinguished after resetting the Card Tester, a true input fault is present in the card-under-test and should be corrected before continuing.

e. Select the output pin to be tested on the front panel IN/OUT SELECTOR switches (S2 and S3). Figure 2 shows a typical example of an output pin (pin 16) and its location on the waveform chart.

f. Set WAVEFORM TEST switch A to the first number shown under the SWITCH SETTING heading which corresponds to the selected output pin on the waveform chart. As shown in figure 2, the number 1 would be selected by switch A.

g. Place WAVEFORM TEST switch B to the first number adjacent to SWITCH SETTING B which corresponds to the selected output pin.

h. Observe the three TEST indicators on the front panel and determine the outcome of the circuit being tested. The two possible indications are explained below:

1. GO indicator lights green - circuit being tested checks good for this measurement and the operator should continue with the next step.

2. NO-GO indicator lights red - circuit being tested does not meet the output requirements for the programmed test. Recheck the switch settings to ensure that there has been no operator error and then make the necessary notations on the card in teat paper work for follow-up maintenance.

i. Place WAVEFORM TEST switches A and B to the next pair of SWITCH SETTINGS, shown on the waveform chart, and observe the TEST indicators as in the previous step. Continue this procedure until all settings for a given OutPut pin have been carried out and all test indications have been GO.

Note

A # symbol in the last "B" switch setting position indicates that a NO-GO indication should be observed for all "B" switch settings (1 through 12). A GO indication in any of these positions indicates a malfunction (more edges than required).

j. Change both IN/OUT SELECTOR switches to the next output pin number located on the waveform chart either adjacent to the output just tested or, if there is no adjacent number, to the next output pin number directly below the output pin just tested.

k. Place WAVEFORM TEST switches A and B to each pair of corresponding SWITCH SETTING numbers. Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO. Repeat steps (j.) and (k.) until all output pins and corresponding SWITCH SETTINGS have been tested.

1. Rotate the card reader handle counter-clockwise to the full open position, remove the program card from the card reader slot and insert the test card into the appropriate plastic card holder.

m. Determine whether or not the card under test requires additional testing using another program test card. If additional testing is required, repeat steps (a.) through (m.) for the additional test (s). If no further testing is required, remove the tested printed circuit card from the card adapter.

MODEL ICT-103 OPERATING PROCEDURES

Following is the step-by-step procedure for performing dynamic test analysis on printed circuit cards programmed for the model ICT-103 Card Tester. These instructions pertain to all printed circuit cards: specific instructions peculiar to individual printed circuit cards undergoing tests are listed as notes on the appropriate waveform sheet. Waveform sheets for individual printed circuit cards are contained in this volume. Before proceeding with any test, the operator must read the notes contained on the waveform sheet and follow any specific instructions first. In addition the necessary card adapters, card extender cables, and programmable load boards should be inserted in the Card Tester to accommodate the card to be tested. The steps listed below provide the necessary information for successful diagnostic testing of all printed circuit cards programmed for testing with the ICT-103.

a. Refer to the appropriate card under test schematic or logic diagram and corresponding waveform sheet, On the waveform sheet, locate the notes and follow the instructions pertinent to the operator. Test notes are normally located along the bottom edge of the waveform sheet.

b. Insert the PC card adapter and/or extender cable (if required) into the CARD IN TEST connector on the front panel of the Card Tester.

C. Insert the printed circuit card to be tested into the card adapter with the component side facing up.

d. Locate the corresponding card-under-test program card and insert it into the card reader slot as depicted on the front panel of the Card Tester. Push the program card into the card reader slot until there is a noticeable resistance felt against the test card. Move the card reader handle clockwise until it is in the full closed position.

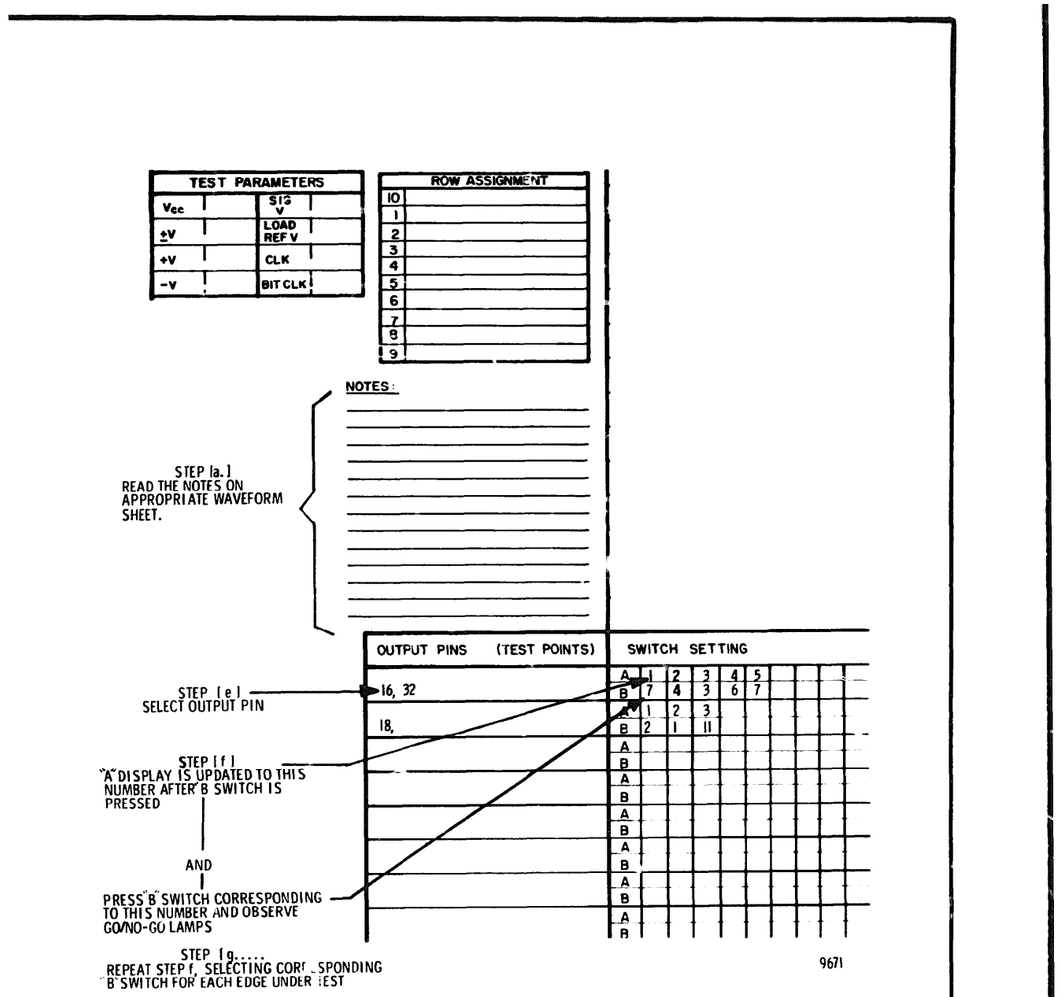


Figure 3. Model ICT-103 Waveform Sheet Example

Note

If the INPUT FAULT indicator is lit, press the RESET switch. If the INPUT FAULT indicator is not extinguished after resetting the Card Tester, a true input fault is present in the card-under-test and should be corrected before continuing.

e. Select the output pin to be tested on the front panel IN/OUT SELECTOR switches (S2 and S3). Figure 3 shows a typical example of an output pin (pin 16) and its location on the waveform chart.

f. WAVEFORM TEST “A” display should read 0 (left digit blank). If the “A” display does not read zero, press the reset switch/indicator.

g. Press the WAVEFORM TEST “B” switch corresponding to the first number adjacent to SWITCH SETTING B (figure 3) which corresponds to the selected output pin (switch number 7 in this example). WAVEFORM TEST display “A” changes to (01).

h. Observe the three TEST indicators on the front panel and determine the outcome of the circuit being tested. The two possible indications are explained below:

1. GO indicator lights green - circuit being tested checks good for this measurement and the operator should continue with the next step.

2. NO-GO indicator lights red - circuit being tested does not meet the output requirements for the programmed test. Recheck the switch settings to ensure that there has been no operator error and then make the necessary notations on the card in test paper work for follow-up maintenance.

i. Press WAVEFORM TEST switch B which corresponds to the next B SWITCH SETTING, shown on the waveform chart, and observe the TEST indicators as in the previous step. Each time a B switch is press the A display is incremented one count. Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO.

j. Change both IN/OUT SELECTOR switches to the next output pin number located on the waveform chart either adjacent to the output just tested or, if there is no adjacent number, to the next output pin number directly below the output pin just tested.

Note

A # symbol ‘in the last “B” switch setting position indicates that a GO test result should occur after “B” switch "#” is depressed. If a NO-GO indication is observed after pressing “B” switch “#“, the circuit being tested has malfunctioned.

k. Press WAVEFORM TEST switch B for each pair of corresponding SWITCH SETTING numbers. Continue this procedure until all settings for a given output pin have been carried out and all test indications have been GO, Repeat steps (j.) and (k.) until all output pins and corresponding SWITCH SETTINGS have been tested.

l. Rotate the card reader handle counter-clockwise to the full open position, remove the program card from the card reader slot and insert the test card into the appropriate plastic card holder.

m. Determine whether or not the card under test requires additional testing using another program test card. If additional testing is required, repeat steps (a.) through (m.) for the additional test (s). If no further testing is required, remove the tested printed circuit card from the card adapter.

Note

In some instances, the GO/NO-GO test documentation may skip "A" display counts to enable the operator to ignore "don't care" transitions in the waveform under test. For example, consider the following:

A	1	2	3	4	5	6	7
B	6	9	NT	NT	3	6	10

Where NT = NO TEST

The operator would press the "B" switches in the following sequence: B-6 (A=1), B-9 (A=2), B-3 three times (steps A to count 5) B-6 (A=6), B-10 (A=7).

SPECIAL CONSIDERATIONS

JUMPERS

Jumpers are required occasionally while performing tests on printed circuit cards for bypassing passive components or otherwise routing DC voltages within the card-under-test. These jumpers should be carefully placed on the card-under-test prior to inserting the program card (energizing the Card Tester) into the Card Tester and should be checked to ensure proper placement. Information concerning placement of jumpers is located in the notes at the bottom of the appropriate waveform test diagram and on the schematics or logic diagrams.

+5V EXT POWER SUPPLY ADJUSTMENT

Four power supply output voltages are available in the Card Tester which can be applied to the card-under-test. Three of these power supplies are controlled by the program test card and the fourth, the +5 Volt EXT power supply,. is adjusted by the operator according to the individual test programs. When adjusting the +5V EXT power supply to accommodate different printed circuit card families, care should be taken to adjust the output voltage within -+100 millivolts of the recommended voltage. Exceeding the 100 millivolt tolerance can cause erroneous readings on the Card Tester GO/NO-GO indicators, as described below.

Erroneous readings caused by maladjusted power supply voltages is normally due to the RC timing circuits present on many cards. A large voltage variation in either direction will cause a significant change in the duration of the timed interval, and may result in an erroneous "B" switch count. This phenomena is illustrated in Figure 4, along with the timing variations imposed by the tolerances on the resistor and capacitor values. The curves were generated for the circuit shown in figure 4. The switching threshold of gate Y was found

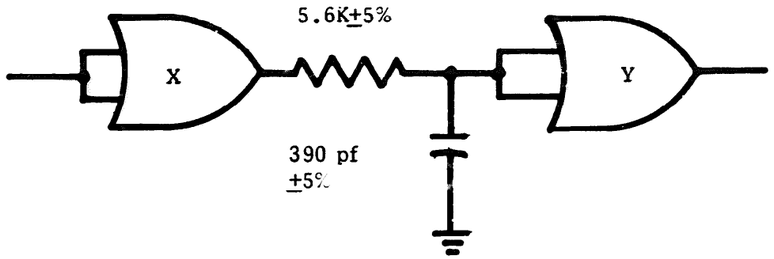


Figure 4. Typical RC Network

to remain nearly constant at approximately 2.0 volts as the supply voltage was varied from 4.50 to 5.00 volts.

It is seen Figure 5 that with Vcc = 4.75 and nominal RC values, Gate Y will switch 1.68 usec after the output of Gate X goes to the high state. With VCC = 5.00 and the resistor and capacitor values at the low end of the tolerance range, Gate Y will delay 1.43 usec before switching. With Vcc = 4.50 and the timing components at the high end of the tolerance range, Gate Y will delay 2.05 usec before switching. Thus, it is seen that for curves A and B, a “B” switch count of 2 would be obtained: while an erroneous “B" switch count of 3 would be obtained for the conditions represented by curve C.

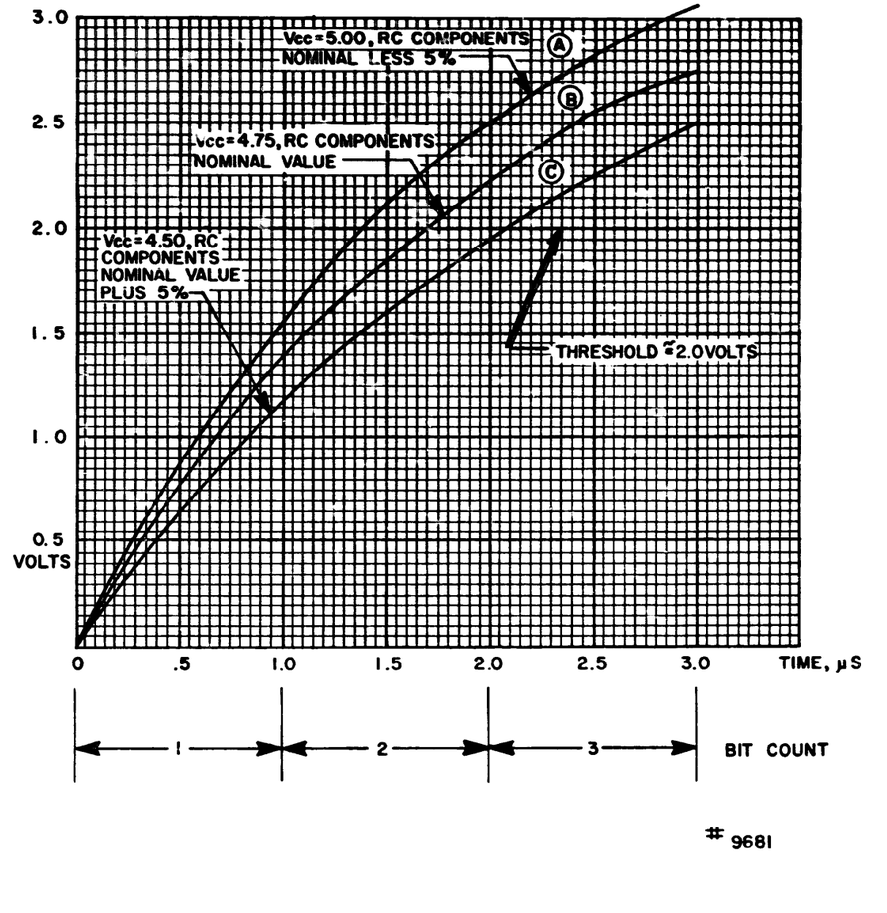


Figure 5. Voltage Tolerance Versus Time Delay Chart

For cases where the time delay circuit is isolated from other circuitry it would usually be possible to program around the problem discussed above. However on many cards, several timing circuits operate in series such that while one programming technique may provide a wide margin of safety for one circuit in the series, it may reduce the margin of safety for another timing circuit in the series. Therefore it is desirable to reduce the magnitude of error of the controllable variables such as supply voltage which determine the duration of the timed intervals.

Note

The above conditions also affect the pulse duration of slivers (spikes) noted in some program waveforms. These spikes are not tested by the Card Tester (too narrow for detection) and are not critical with respect to the logic circuit operation. In most cases the spikes are less than 10 nanoseconds in duration and in some cases are hardly discernable from one Card Tester to the next.

PRINTED CIRCUIT CARD ADAPTERS

Several printed circuit card adapters are available to interconnect between the Card Tester and various printed circuit card families contained in this manual. Following is a cross-reference table of the individual card adapters and associated printed circuit card family, Pin number cross-reference and card adapter identification for individual PC card adapters are provided in the following tables and illustrations.

Table 1. Printed Circuit Card Adapters

DYNATRONICS PART NO.	MILITARY NOMENCLATURE	ADAPTS CARD TESTER TO:
12-890051	MX-9089/USM-371.	23 Pin Anelex
12-890052	MX-9090/USM-371.	44/88 Pin Anelex
12-890053	MX-9091/USM-371	22 Pin SN-394 (RED)
12-890054	MX-9092/USM-371.	26 Pin SN-394 (BLACK)
12-890056	MX-9093/USM-371.	22 Pin MD-674
12-890059	MX-9094/USM-371.	43/86 Pin FGC
12-890055	MX-9095/USM-371.	60 Pin TCU
12-890050	MX-9096/USM-371.	46 Pin GDE
12-890058	MX-9097/USM-371.	25 Pin FGC

Table 2. Printed Circuit Card Adapter MX-9089/USM-371
Pin Cross reference

ADAPTER MX-9089/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9089/USM-371	CARD TESTER PIN NUMBER
1	46	12	35
2	45	13	34
3	44	14	33
4	43	15	32
5	42	16	31
6	41	17	30
7	40	18	29
8	39	19	28
9	38	20	27
10	37	21	26
11	36	22	25
		23	24

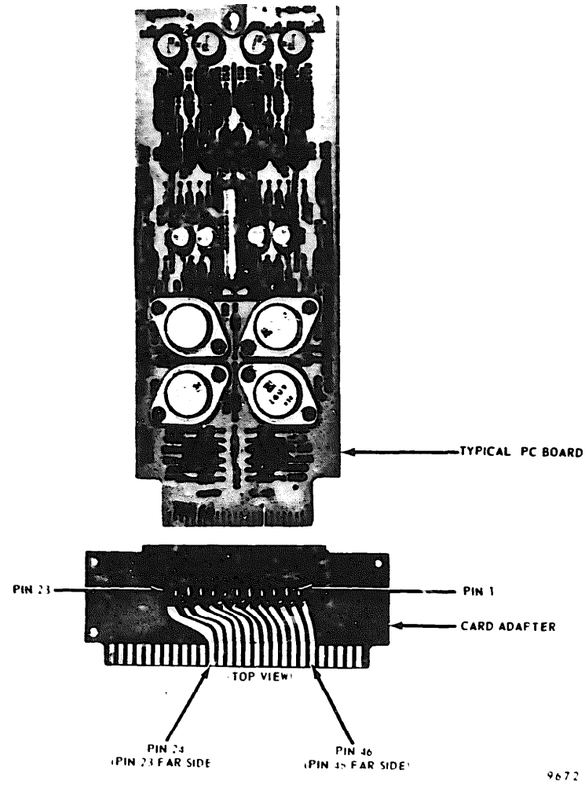


Figure 6. Printed Circuit Card Adapter MX-9089/USM-371
(23 Pin Anelex)

Table 3. Printed Circuit Board Adapter MX-9090/USM-371
Pin Cross Reference

ADAPTER MX-9090/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9090/USM-371	CARD TESTER PIN NUMBER
1	55	23	36
2	53	24	34
3	51	25	32
4	49	26	30
5	47	27	28
6	45	28	26
7	43	29	24
8	41	30	22
9	39	31	20
10	37	32	18
11	35	33	16
12	33	34	14
13	31	35	12
14	29	36	10
15	52	37	8
16	50	38	6
17	48	39	4
18	46	40	2
19	44	41	54
20	42	42	
21	40	43	56
22	38	44	

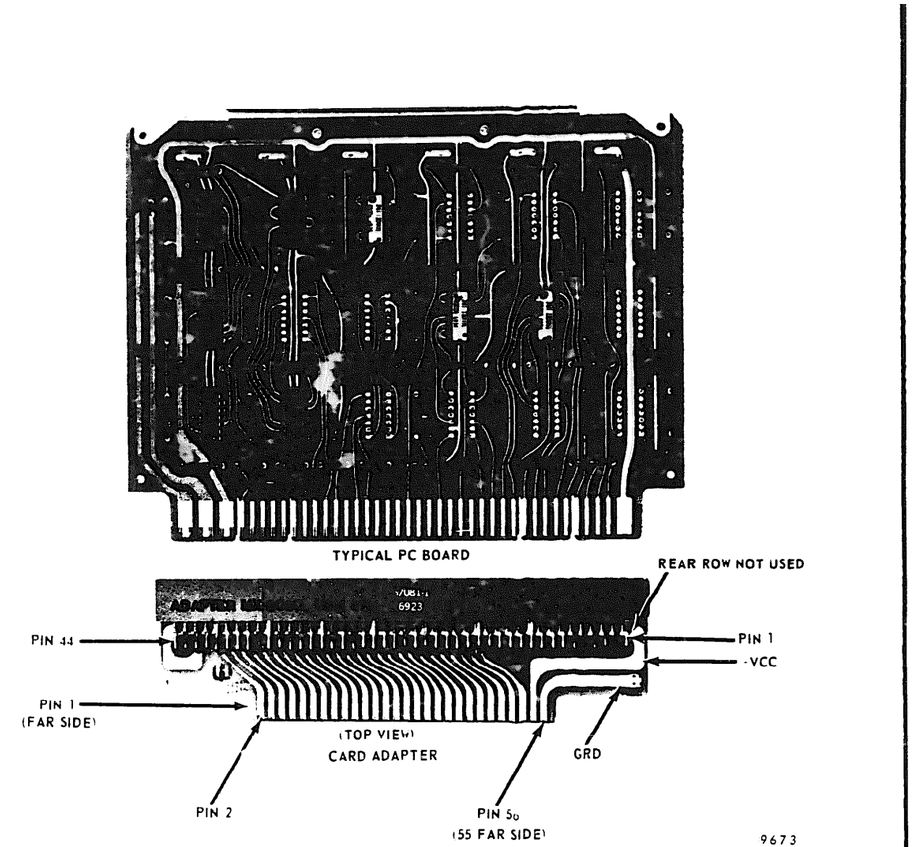


Figure 7. printed Circuit Card Adapter MX-9090/USM-371
(44/88 Pin Anelex)

Table 4. Printed Circuit Card Adapter MX-9091/USM-371
Pin Cross References

ADAPTER MX-9091/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9091/USM-371	CARD TESTER PIN NUMBER
1	22	12	11
2	21	13	10
3	20	14	9
4	19	15	8
5	18	16	7
6	17	17	6
7	16	18	5
8	15	19	4
9	14	20	3
10	13	21	2
11	12	22	1

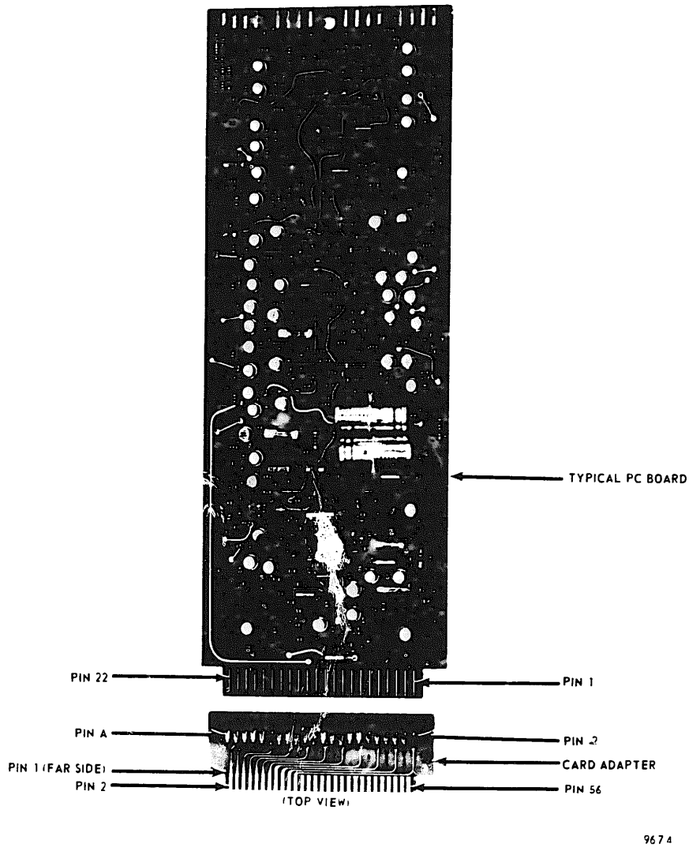


Figure 8, Printed Circuit Card Adapter MX-9091/USM-371
22 Pin SN-394 (Red)

Table 5. Print Circuit Card Adapter MX-9092/USM-371
Pin Cross Reference

ADAPTER MX-9092/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9092/USM-371	CARD TESTER PIN NUMBER
1	52	29	26
2	51	30	25
3	50	31	24
4	49	32	23
5	48	33	22
6	47	34	21
7	46	35	20
8	45	36	19
9	44	37	18
10	43	38	17
11	42	39	16
12	41	40	15
13	40	41	14
14	39	42	13
15	38	43	12
16	37	44	11
17	36	45	10
18	35	46	9
19	34	47	8
20	33	48	7
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24	29	52	3
25	28	53	2
26	27	54	1

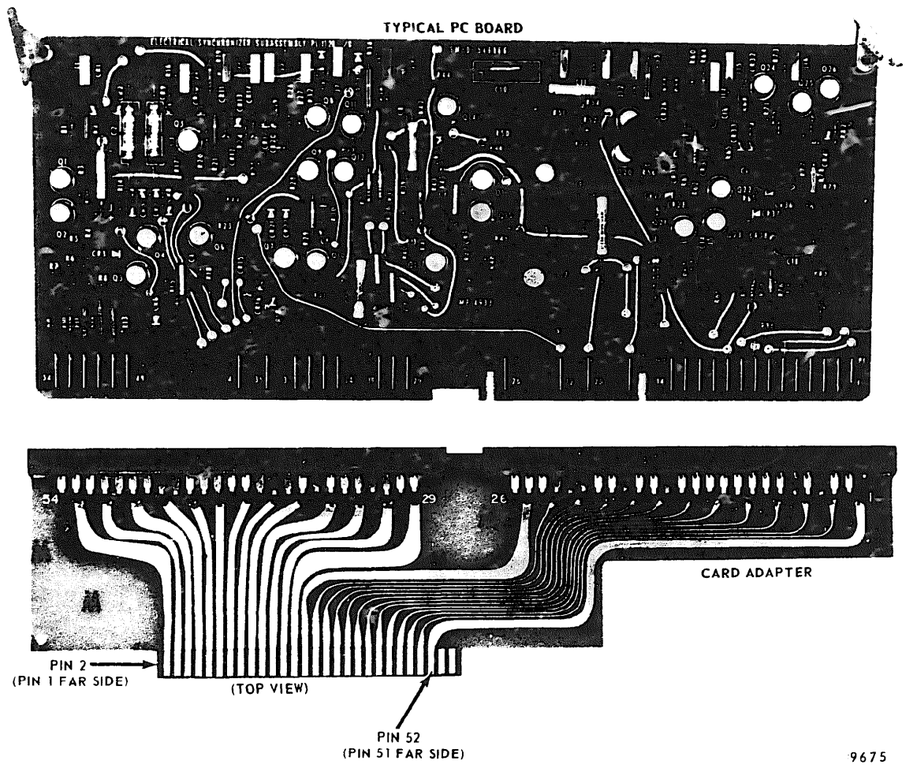


Figure 9. Printed Circuit Card Adapter MX-9092/USM-371
26 Pin SN-394 (Black)

Table 6. Printed Circuit Card Adapter MX-9093/USM-371
Pin Cross Reference

ADAPTER MX-9093/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9093/USM-371	CARD TESTER PIN NUMBER
A	1	N	12
B	2	P	13
C	3	R	14
D	4	S	15
E	5	T	16
F	6	U	17
H	7	V	18
J	8	W	19
K	9	X	20
L	10	Y	21
M	11	Z	22

#G, I, O, Q - omitted

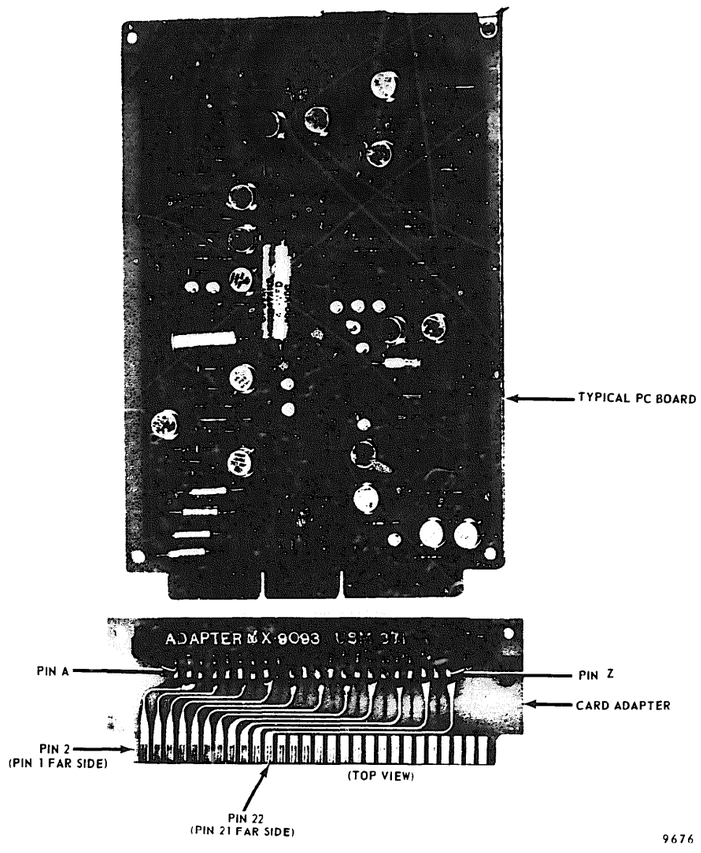


Figure 10. Printed Circuit Card Adapter MX-9093/USM-371
22 Pin MD-674

Table 7. Printed Circuit Card Adapter MX-9094/USM-371
Pin Cross Reference

ADAPTER MX-9094/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9094/USM-371	CARD TESTER PIN NUMBER
1	1	45	23
3	2	47	24
5	3	49	25
7	4	51	26
9	5	53	27
11	6	55	28
13	7	57	29
15	8	59	30
17	9	61	31
19	10	63	32
21	11	65	33
23	12	67	34
25	13	69	35
27	14	71	36
29	15	73	37
31	16	75	38
33	17	77	39
35	18	79	40
37	19	81	41
39	20	83	42
41	21	85	43
43	22		

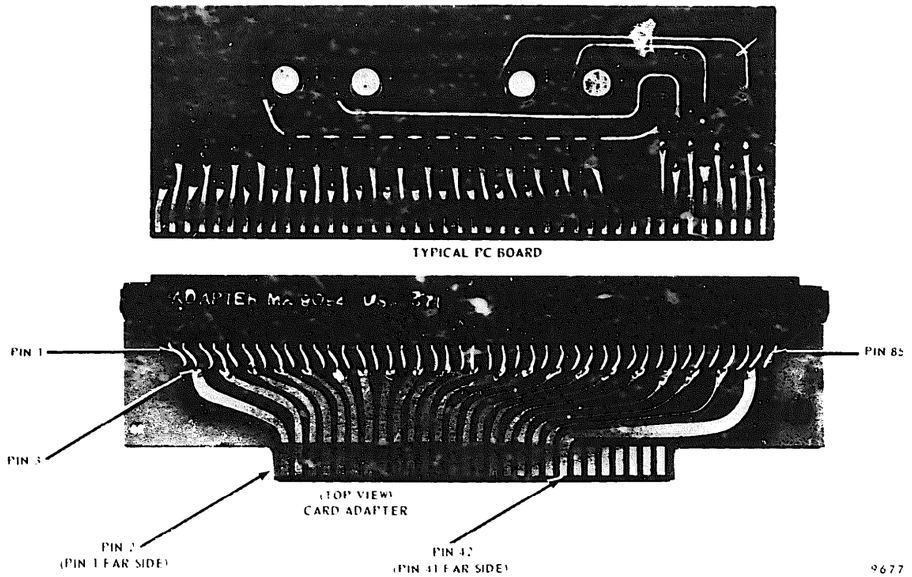


Figure 11. Printed Circuit Card Adapter MX-9094/USM-371
43/86 Pin FGC

Table 8. Printed Circuit Card Adapter MX-9095/USM-371
Pin Cross Reference

ADAPTER MX-9095/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9095/USM-371	CARD TESTER PIN NUMBER
1	56	31	54 (+5V)
2	51	32	No connection
3	No connection	33	55
4	49	34	53
5	47	35	52
6	45	36	50
7	43	37	48
8	41	38	46
9	39	39	44
10	37	40	42
11	35	41	40
12	33	42	38
13	31	43	36
14	29	44	34
15	27	45	32
16	25	46	30
17	23	47	28
18	21	48	26
19	19	49	24
20	17	50	22
21	15	51	20
22	13	52	18
23	11	53	16
24	9	54	14
25	7	55	12
26	5	56	10
27	3	57	8
28	No connection	58	6
29	No connection	59	4
30	1	60	2

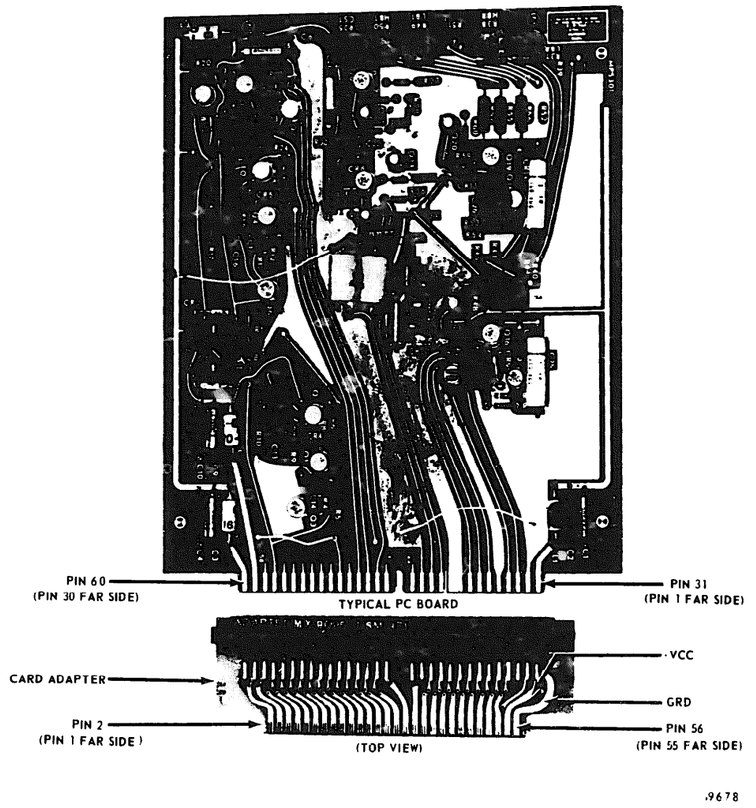


Figure 12. Printed Circuit Card Adapter MX-9095/USM-371
60 Pin TCU

Printed Circuit Card Adapter MX-9096/USM-371
Pin Cross Reference

ADAPTER MX-9096/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9096/USM-371	CARD TESTER PIN NUMBER
*1	55	A	56 (GRD.)
*2	53	B	54(+4.75V)
3	51	C	52
4	49	D	50
5	47	E	48
6	45	F	46
7	43	H	44
8	41	J	42
9	39	K	40
10	37	L	38
11	35	M	36
12	33	N	34
13	31	P	32
14	29	R	30
15	27	S	28
16	25	T	26
17	23	U	24
18	21	V	22
19	19	W	20
20	17	X	18
21	15	Y	16
22	13	Z	14
23	11	AA	12

* If these pins are Power/GRD they are tied to +4.5V/GRD on Autodin Card itself.

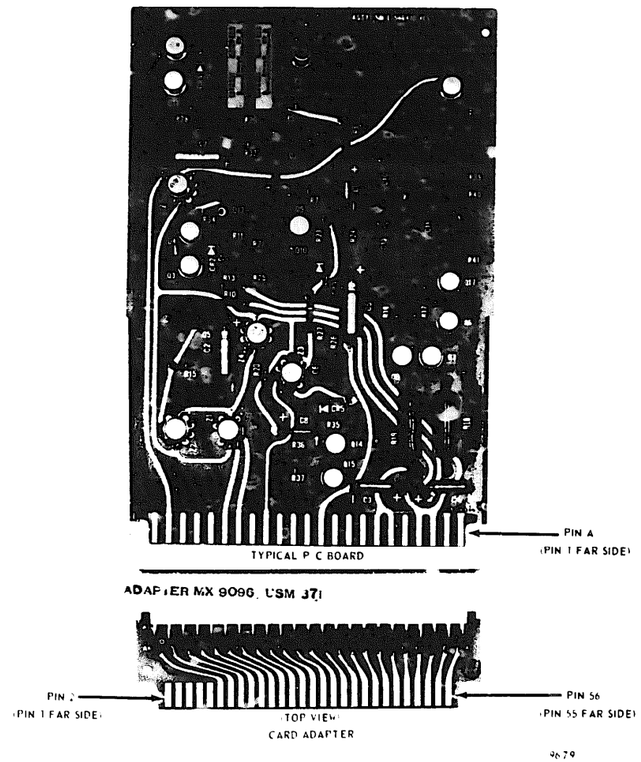


Figure 13. Printed Circuit Card Adapter MX-9096/USM-371
46 Pin GDE

Table 10. Printed Circuit Card Adapter MX-9097/USM-371
Pin Cross Reference

ADAPTER MX-9097/USM-371	CARD TESTER PIN NUMBER	ADAPTER MX-9097/USM-371	CARD TESTER PIN NUMBER
1	25	13	13
2	24	14	12
3	23	15	11
4	22	16	10
5	21	17	9
6	20	18	8
7	19	19	7
8	18	20	6
9	17	21	5
10	16	22	4
11	15	23	3
12	14	24	2
		25	1

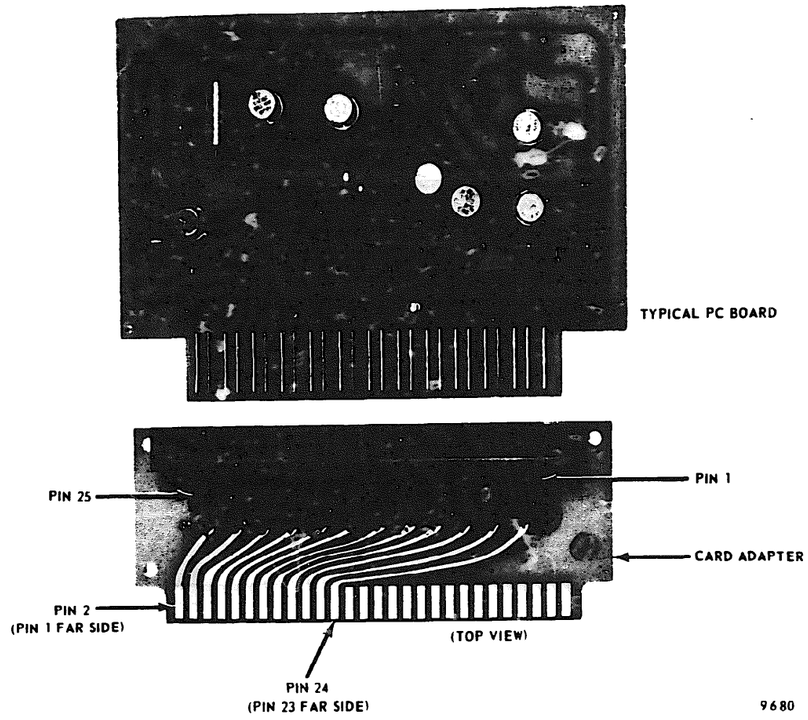
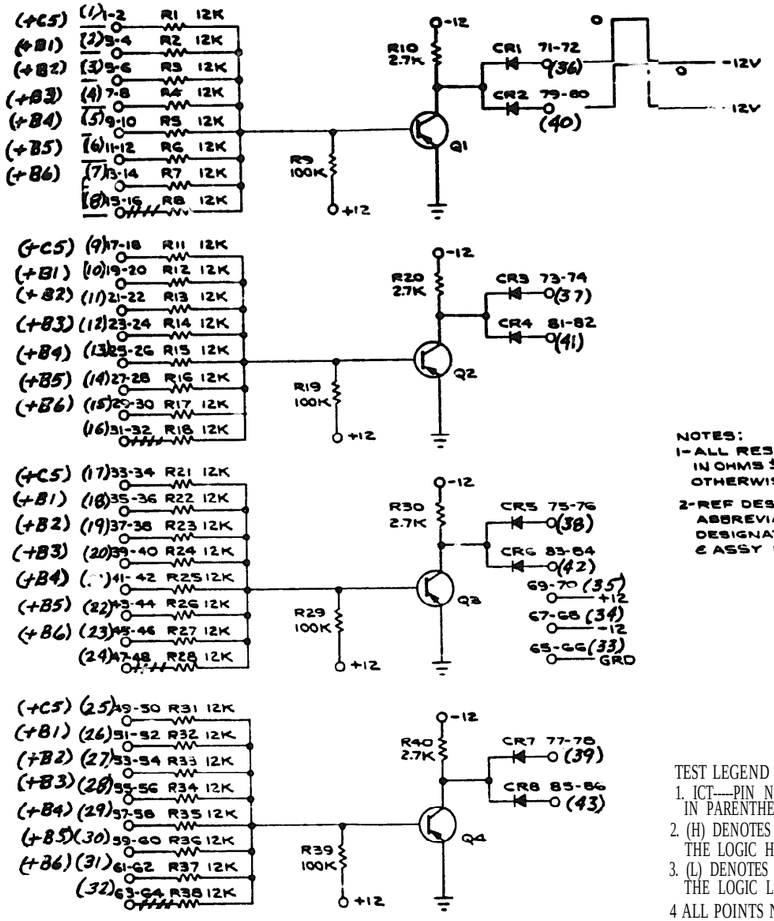


Figure 14. Printed Circuit Card Adapter MX-9097/USM-371
25 Pin FGC



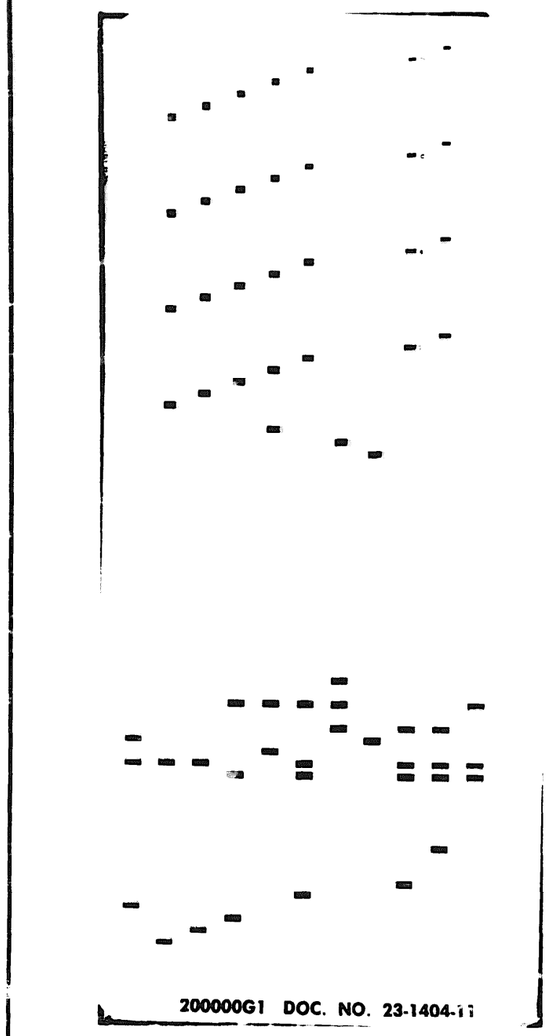
NOTES:
1- ALL RESISTANCE VALUES ARE IN OHMS ± 5% ¼ 1/4 WATT UNLESS OTHERWISE SPECIFIED.

2- REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION.

TEST LEGEND AS APPLICABLE'

1. ICT-----PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e. ARE SWITCHING DURING TEST
5. -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES

JN 7-8-71



200000G1 DOC. NO. 23-1404-11

APPD JN 7-8-71

TEST PARAMETERS

Vcc		SIG V	
5V		LOAD REF V	A
0V		CLK	
V		RST CLR	

ROW ASSIGNMENT

10	+C0
1	+B1
2	+B2
3	+B3
4	+B4
5	+B5
6	+B6
7	+B7
8	+S0
9	+S1

INPUT PINS	COL	SIG
	63	+C0
	64	C1
	65	C2
	66	C3
	67	C4
3, 16, 17, 24	68	+C5
	69	+C6
	70	+B0
9, 10, 18, 26	71	+B1
5, 11, 19, 27	72	+B2
4, 12, 20, 28	73	+B3
13, 21, 29	74	+B4
6, 14, 22, 30	75	+B5
7, 15, 23, 31	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

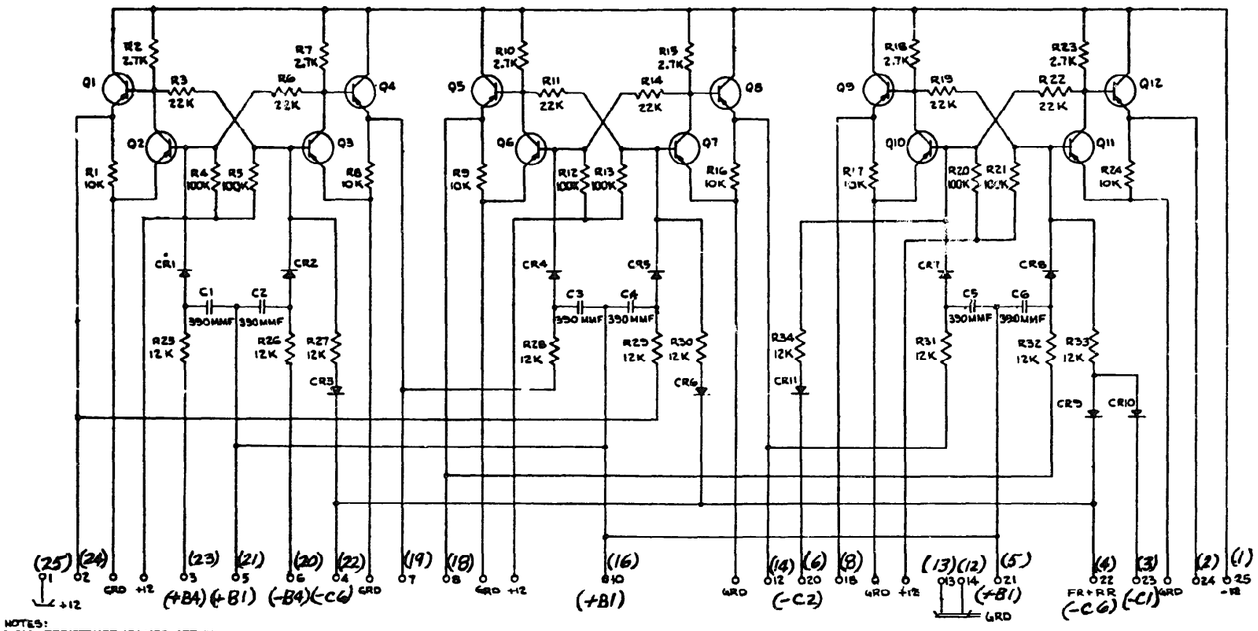
OUTPUT PINS (TEST POINTS) — SWITCH SETTING — +C0 REF

OUTPUT PINS (TEST POINTS)
16, 32
17, 41
38, 42
39 *

WAVEFORMS — ← → 120 µS — DYNATRONICS TESTAGRAM

NOTE:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.



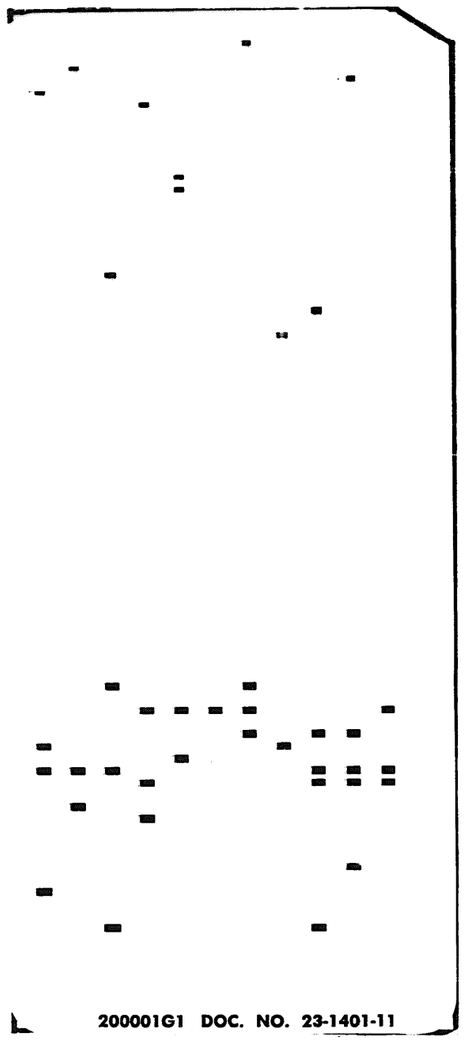
NOTES:
1. ALL RESISTANCE VALUES ARE IN OHMS ±5% ¼ 1/4 WATT UNLESS OTHERWISE SPECIFIED.
2. REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION.

TEST LEGEND AS APPLICABLE.

1. ICT----PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST
5 -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES

7-8-71

JN

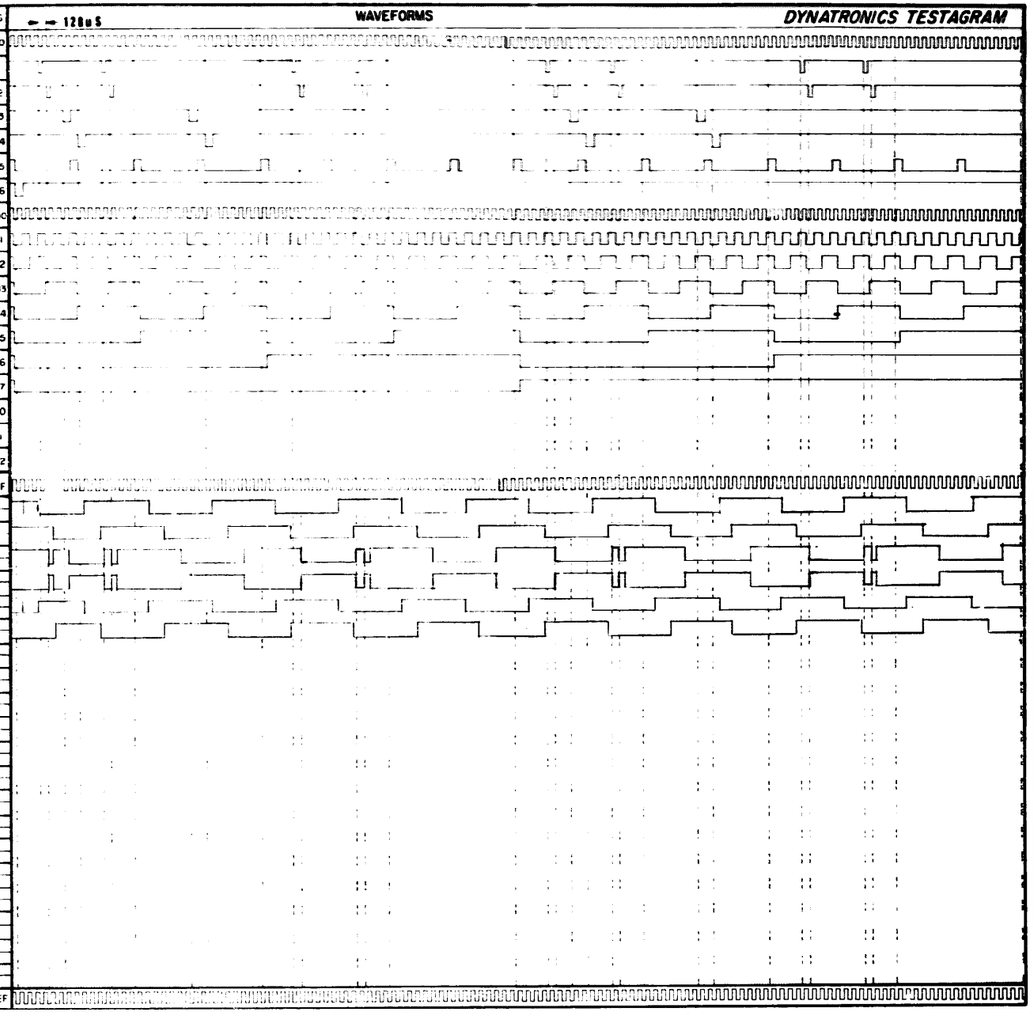


200001G1 DOC. NO. 23-1401-11

TEST PARAMETERS			
Vcc	+4.75	SIG V	@ TP3=-12V
-V	-12V	LOAD REF V	N/A
+V	+12V	CLK	32μ sec
-V	——	SET CLK	+OSC

ROW ASSIGNMENT	
10	-C6
1	+B4
2	+12
3	-12V
4	—
5	GND
6	-C2
7	-B4
8	-C1
9	+B1

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2



OUTPUT PINS (TEST POINTS)	SWITCH SETTING
19	
14	
2	
8	
24	
18	

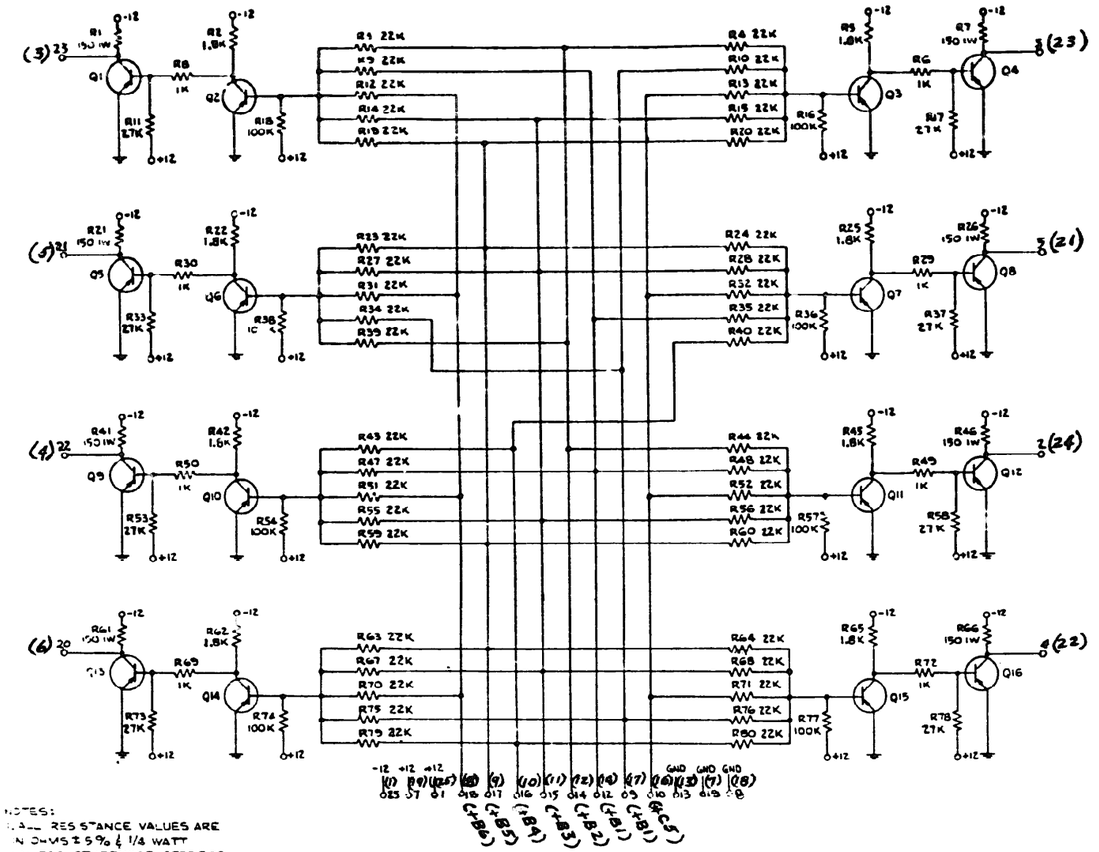
+C0 REF

+B0 REF

NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

APPD. JN 7-A-71



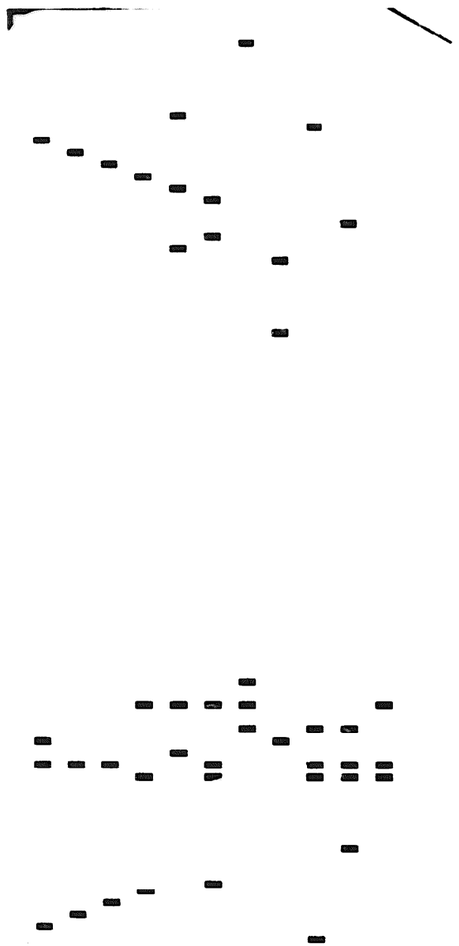
NOTES:
1. ALL RESISTANCE VALUES ARE IN OHMS ± 5% & 1/8 WATT UNLESS OTHERWISE SPECIFIED.
2. REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION.

TEST LEGEND AS APPLICABLE:

1 ICT——PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ⫻ INDICATES UNTESTED INPUT/OUTPUT LINES.

JN 28-71

P.C. Assembly 2 0 0 0 0 0 2 G 1



200002G1 DOC. NO. 23-1403-11

CONT APPD. JW DATE 7-8-71

TEST PARAMETERS			
Vcc +4.75	SIG V	@ -2V	
5V	LOAD REF V		
+V	CLK		
-V	BIT CLK		

ROW ASSIGNMENT	
10	+C5
1	+B0
2	+12 V
3	17 V
4	+B1
5	GND
6	+B2
7	+B3
8	+B4
9	+B5

INPUT PINS	COL	SIG
	63	+C0
	64	C1
	65	C2
	66	+C3
	67	C4
13	68	+C5
	69	C6
	70	+B0
14,17	71	+B1
12	72	+B2
11	73	+B3
10	74	+B4
9	75	+B5
8	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING	+CO REF
22	A 1 2 3 / B 2 6 9	
24	A 1 2 3 4 5 / B 2 7 10 16 9	
21	A 1 2 3 / B 2 6 9	
23	A 1 2 3 4 5 / B 2 7 14 6 9	
6	A 1 2 3 4 5 / B 2 4 8 1 5	
4	A 1 2 3 4 5 / B 2 4 8 1 5	
5	A 1 2 3 4 5 / B 2 2 6 1 5	
3	A 1 2 3 4 5 / B 2 2 6 1 5	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	
	A / B	

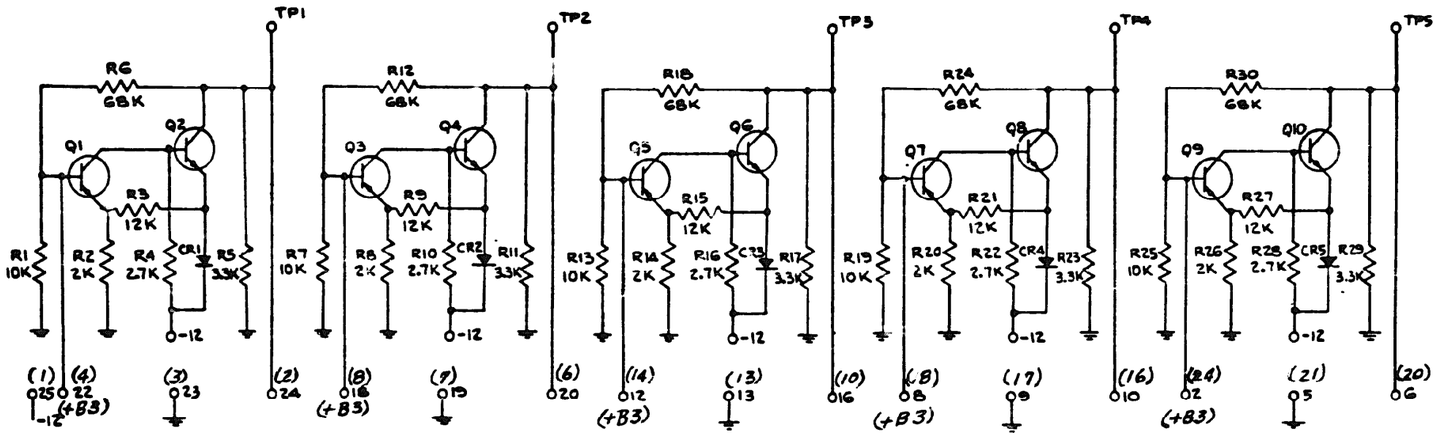
+RO REF

← → 128uS WAVEFORMS DYNATRONICS TESTAGRAM

NOTE :

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

TEST LEGEND AS APPLICABLE:
1 ICT----PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHiNG DURING TEST.
5 -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES.

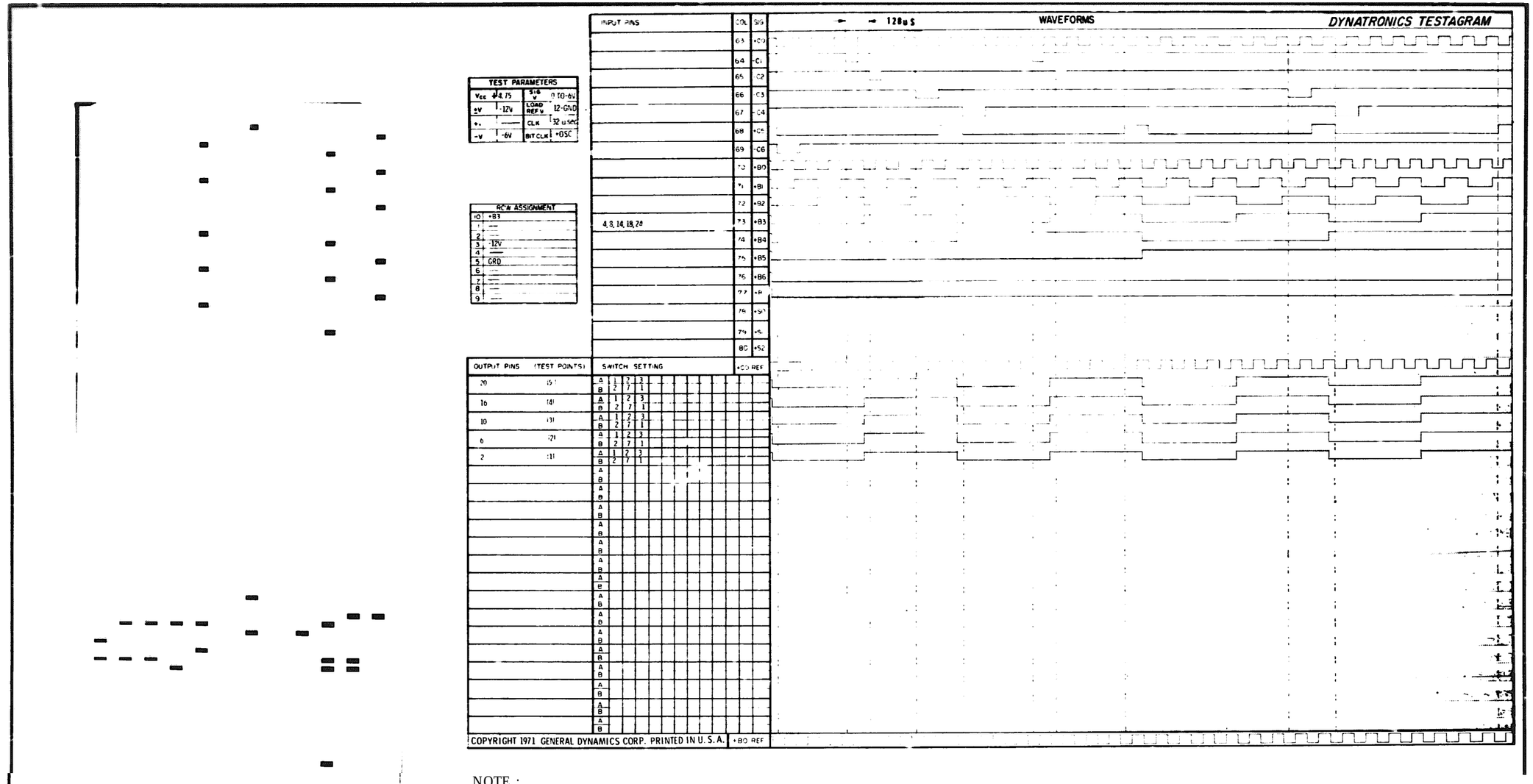


NOTES:
1.ALL RESISTANCE VALUES ARE IN OHMS ± 5% ½ 1/4 WATT UNLESS OTHERWISE SPECIFIED.
2.REF DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION.

JN 7-8-71

P.C. Assembly 200003 G1

P. C. Logic Doc. No. 23-1402-11

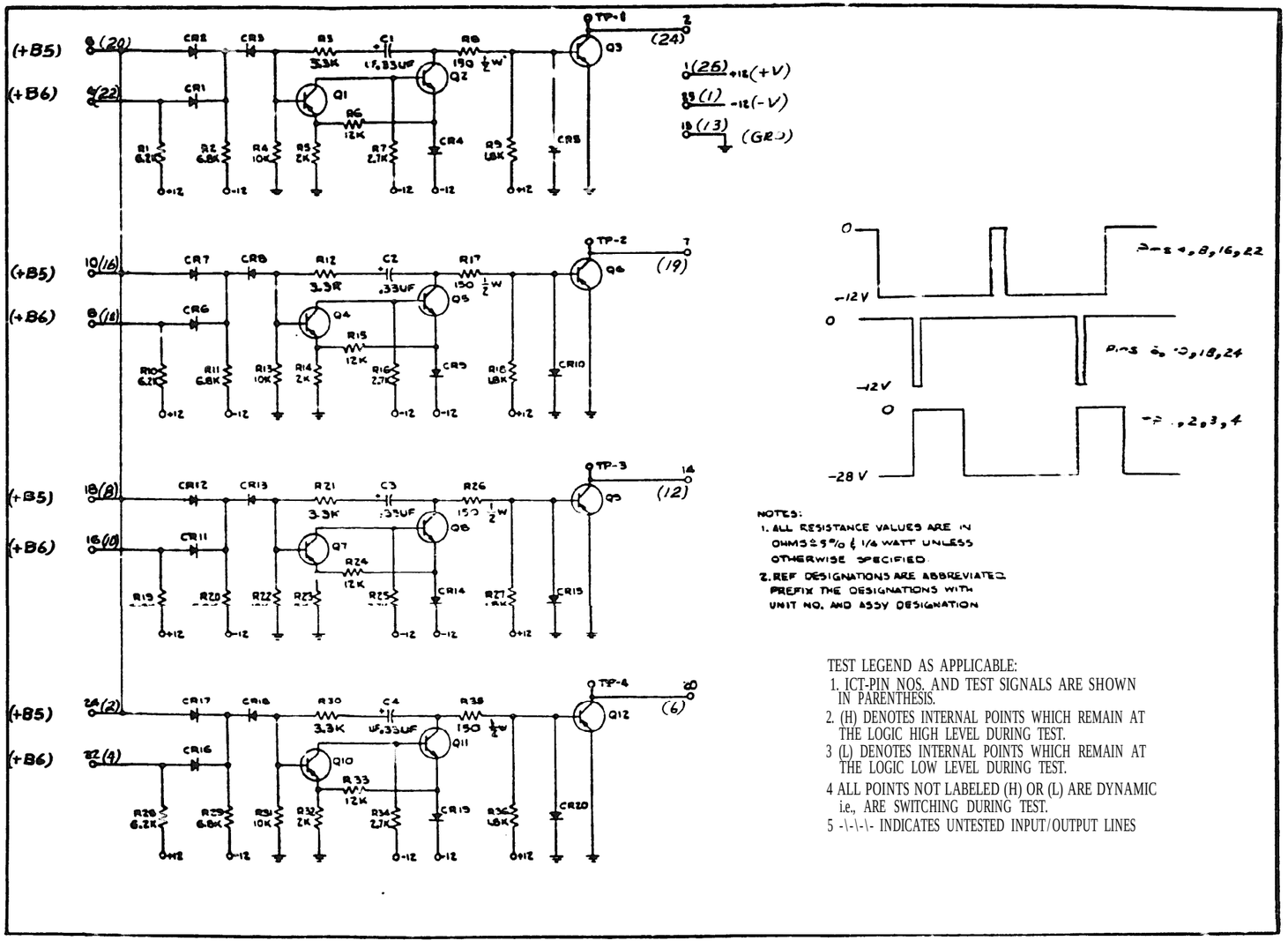


200003G1 DOC. NO. 23-1402-11

UNIT APPD. JN DATE 7-8-71

NOTE :

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.



NOTES:
1. ALL RESISTANCE VALUES ARE IN OHMS ±5% & 1/4 WATT UNLESS OTHERWISE SPECIFIED.
2. REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION

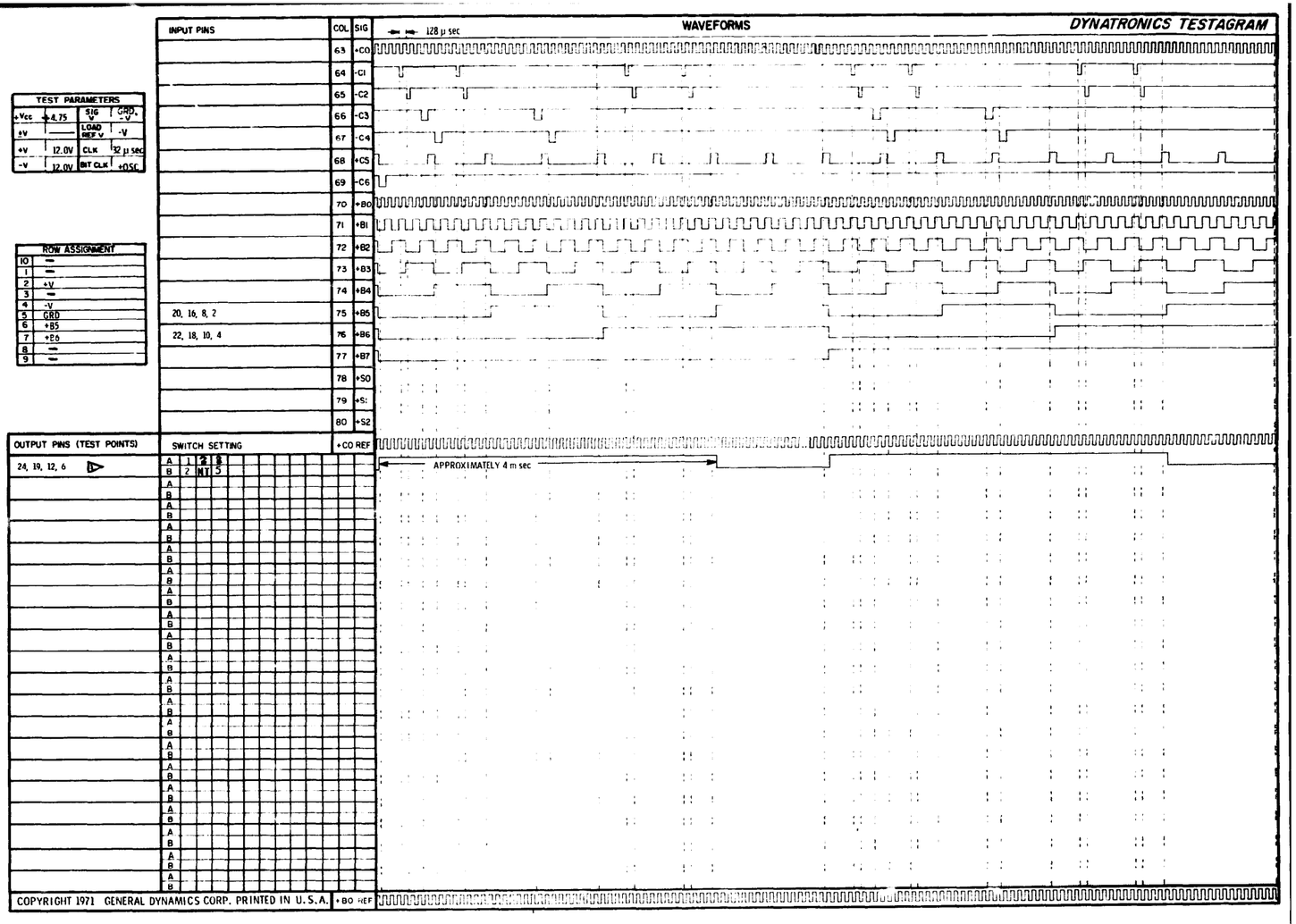
TEST LEGEND AS APPLICABLE:

1. ICT-PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5 -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES

JN 7-8-71

P.C. Assembly 200004G1

P.C. Logic NAVSHIPS 0967 216 3010 Doc. No. 23- 2616-11
Fig. 5-32



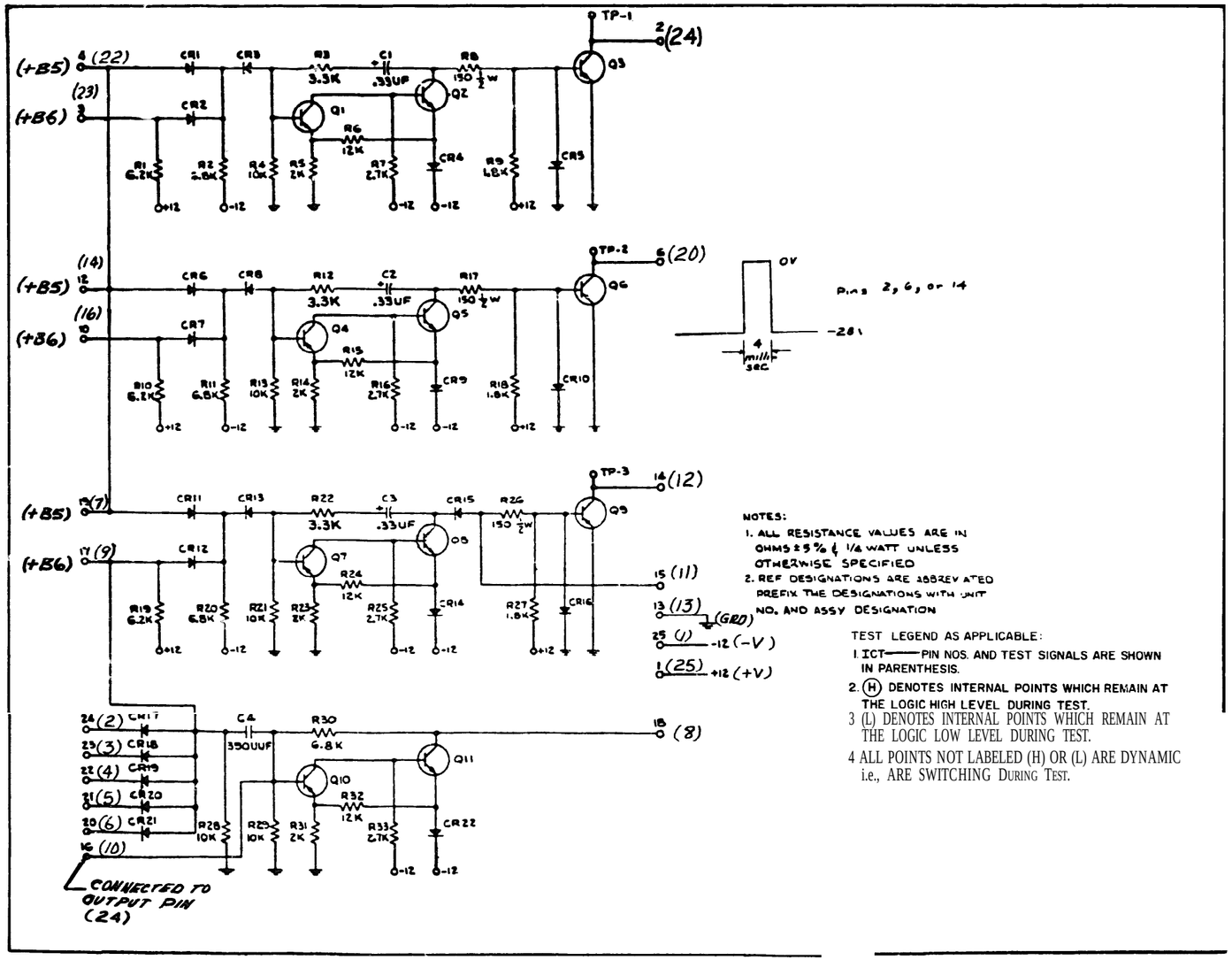
NOTE:

1. BECAUSE OF THE VARIATIONS IN MONOSTABLE "ON" TIME, ONLY THE LEADING EDGE IS GO/NO-GO TESTED.

2. NT INDICATES NO TEST.

200004G1 DOC. NO. 23-2616-11

DATE 7-8-71



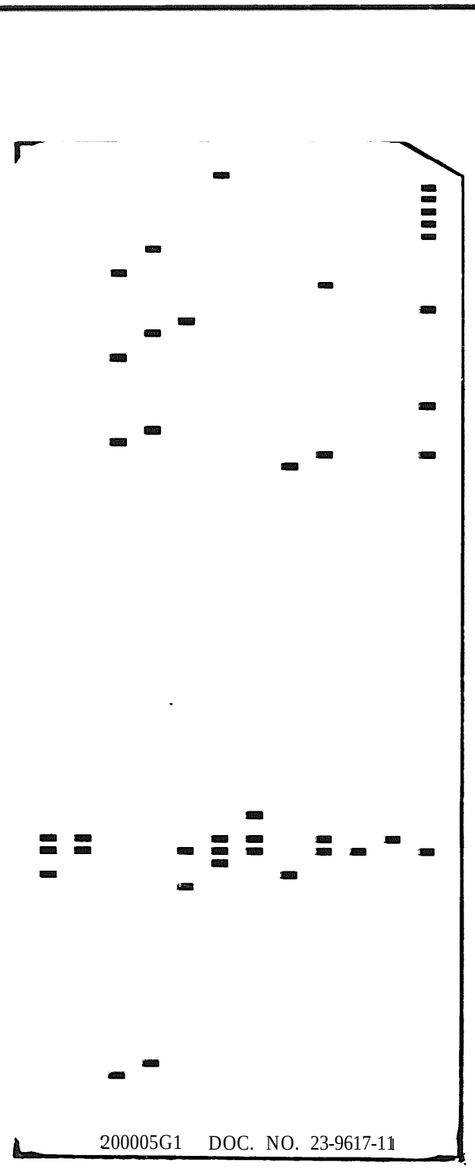
NOTES:
1. ALL RESISTANCE VALUES ARE IN OHMS ±5% @ 1/4 WATT UNLESS OTHERWISE SPECIFIED
2. REF DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION

TEST LEGEND AS APPLICABLE:
1. ICT——PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.

APPD. JN 7-5-71

P. C. Assembly 200005G1

P.C. Logic NAVSHIPS 0967 216 30 10 Doc. No. 23- 2617-11
Fig. 5-33



200005G1 DOC. NO. 23-9617-11

JN 7-8-71

TEST PARAMETERS			
+Vcc	+4.75	SIG V	GRD, -V
±V	—	LOAD REF. V	-V
+V	12.0V	CLK	32 μ sec
-V	12.0V	EXT CLK	+OSC

ROW ASSIGNMENT	
10	—
1	PIN 10 TO PIN 24
2	+V
3	—
4	-V
5	GRD
6	+B5
7	+B6
8	—
9	—

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
22, 14, 7	75	+B5
23, 16, 9	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
SWITCH SETTING		+CO REF

OUTPUT PINS (TEST POINTS)

8, 12, 20, 24, 11* ▽

2, 3, 4, 5, 6

WAVEFORMS — 128 μ sec

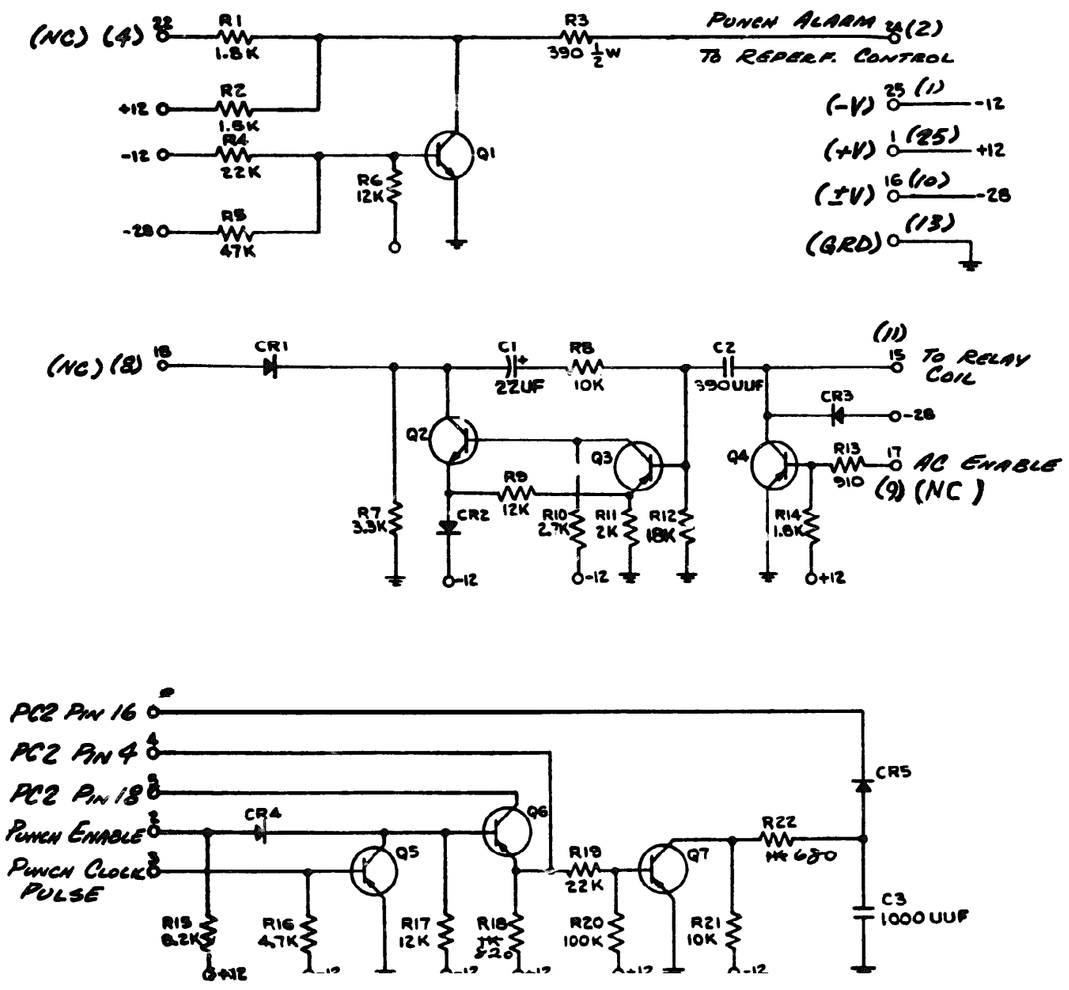
APPROXIMATELY 4 m sec

DYNATRONICS TESTAGRAM

+BO REF

NOTES :

1. * DENOTES INVERTED SIGNAL.
2. BECAUSE OF THE VARIATION IN MONOSTABLE "ON" TIME, ONLY THE LEADING EDGE IS GO/NO-GO TESTED.
3. NT INDICATES NO TEST.



TEST LEGEND AS APPLICABLE:

1. ICT---PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES.
6. THIS TEST APPLIES POWER ONLY.

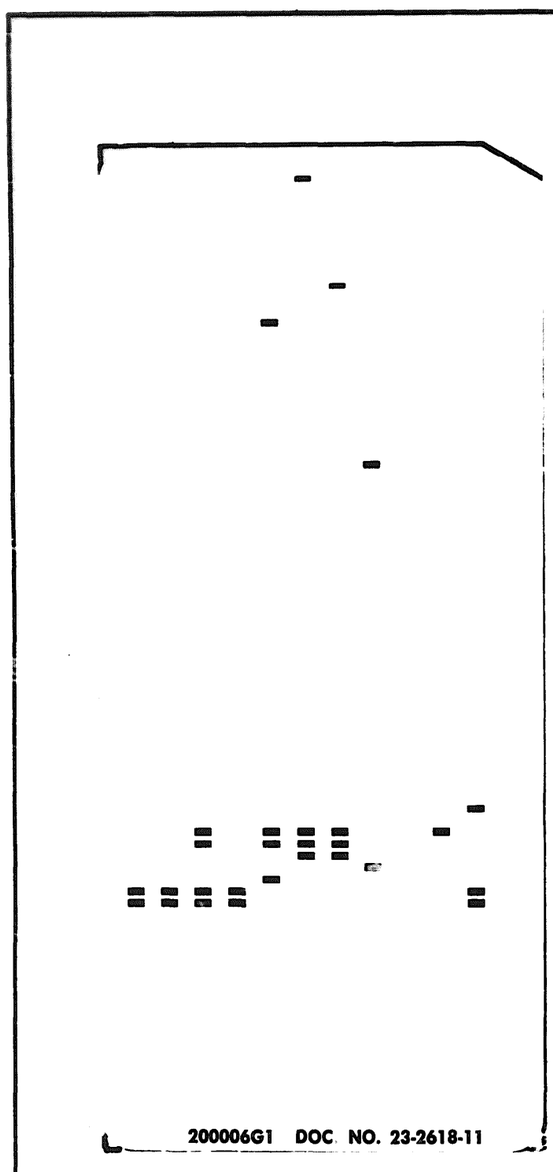
NOTES:

1. ALL RESISTANCE VALUES ARE IN OHMS ±5% AND 1/4 WATT UNLESS OTHERWISE SPECIFIED.
2. REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION.

JN 7-8-71

P.C. Assembly 200006G1

P.C. Logic NAVSHIPS 0967 216 3010 Doc. No. 23-2618-11



200006G1 DOC. NO. 23-2618-11

TEST PARAMETERS			
V_{cc}	+4.75	SIG V	GRD, VIC
-6V	-26.1	LOAD REF V	
+V	12	CLK	
-V	12	BIT CLK	

ROW ASSIGNMENT	
10	
1	
2	+12V
3	-26.1V
4	-12V
5	GRD
6	
7	
8	
9	

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
	+C0 REF	

WAVEFORMS

DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
1	A B

+B0 REF

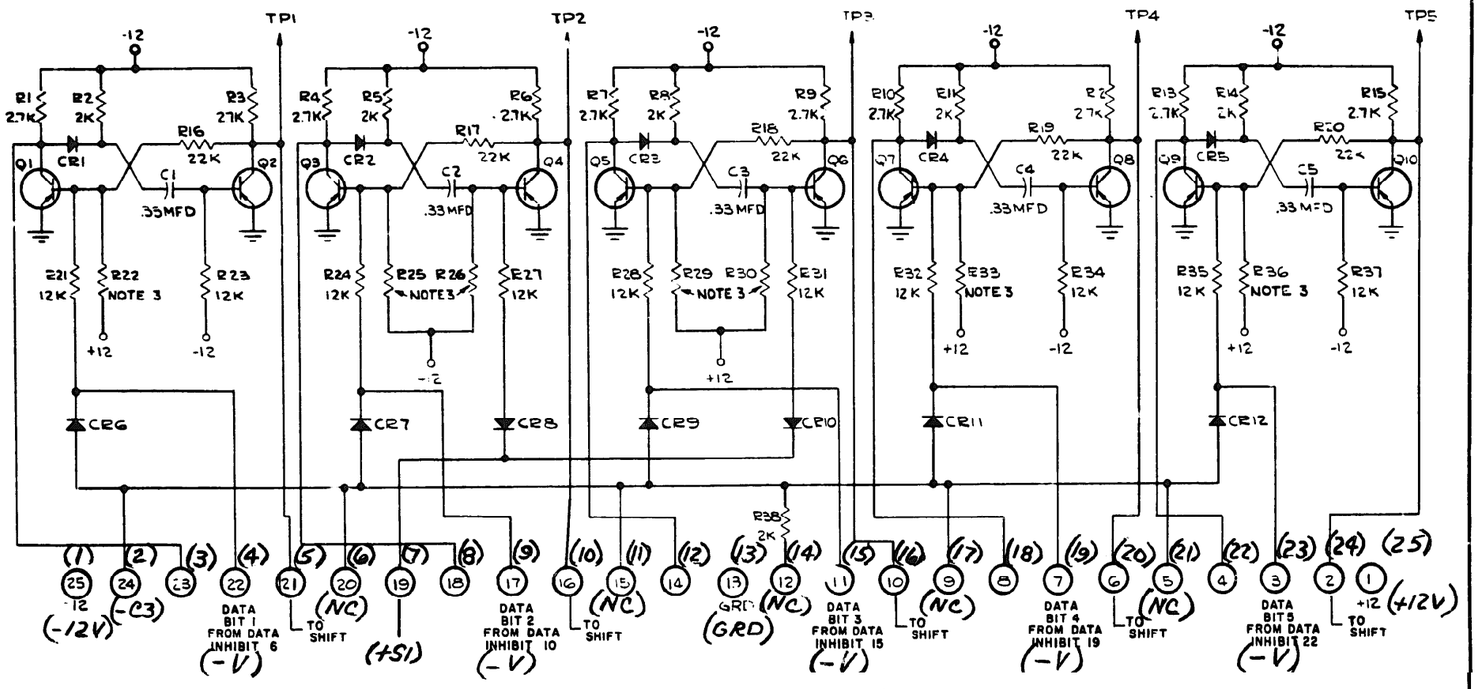
NOTES:

1. THIS TEST APPLIES POWER ONLY.

APPD. JN DATE 7-2-71

NOTES:

1. ALL RESISTANCE VALUES ARE IN OHMS ±5% 1/4 WATT UNLESS OTHERWISE SPECIFIED.
2. REF DESIGNATIONS ARE ABBREVIATED. PREFIX WITH UNIT NUMBER AND ASSEMBLY.
3. 100K VALUE USED IN SYSTEM SERIAL NO. A1 THRU A25 AND 47K IN ALL FOLLOWING SYSTEMS.

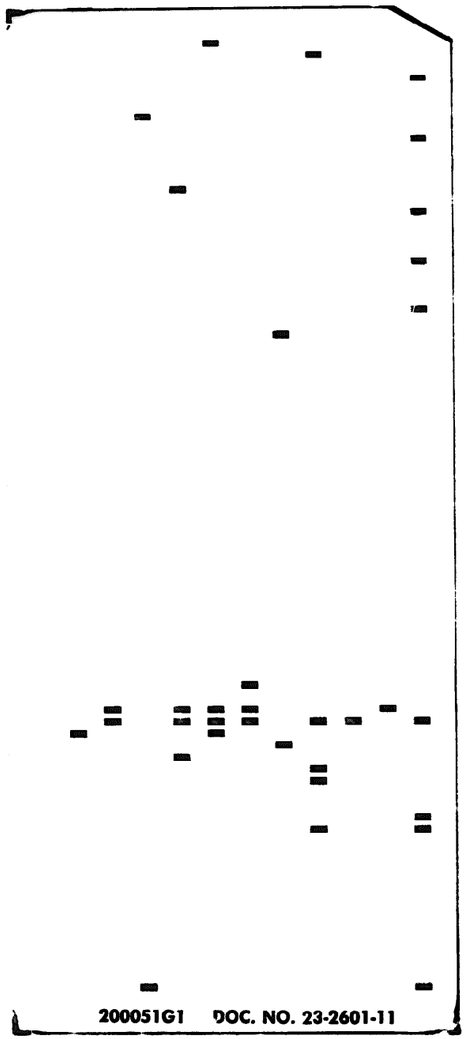


TEST LEGEND AS APPLICABLE:

1. ICT-----PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN At THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST
5. -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES.

P.C. Assembly 200051 G1
P.C. Logic

Doc. No. 23-2601-11



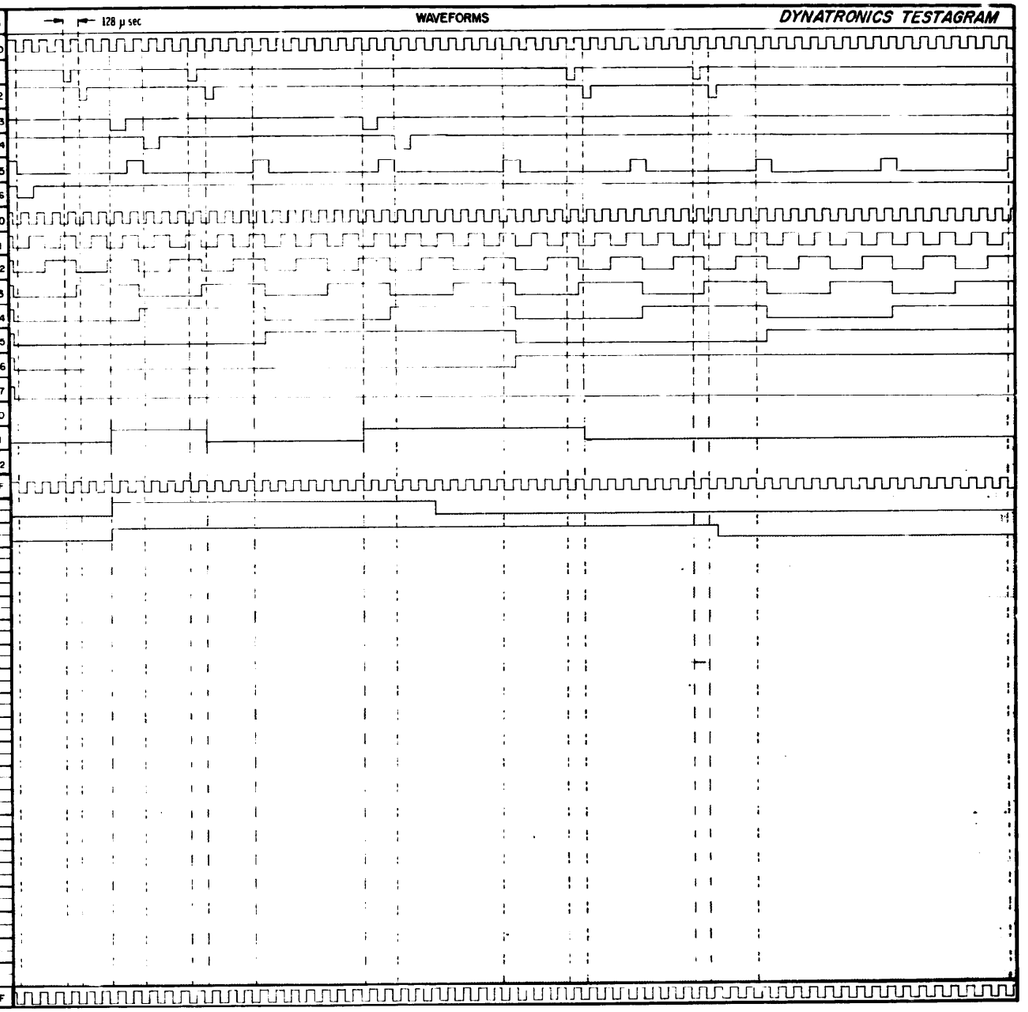
200051G1 DOC. NO. 23-2601-11

TEST PARAMETERS			
$+V_{cc}$	+4.75V	SIG	0V +12V
±V	——	LOAD REF	-V
+V	+12V	CLK	32 µsec
-V	-12V	SET CLR	——

ROW ASSIGNMENT	
10	—
1	-C3
2	+12V
3	—
4	-12V
5	GRD
6	+S1
7	—
8	—
9	—

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
2	66	C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
7	79	+S1
	80	+S2
SWITCH SETTING		+C0 REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
3, 18, 22, 5*, 20*, 24*	A 1 1 1 1 / B 1 1 1 1
8, 12, 10*, 16*	A 1 2 3 / B 1 1 1



+ B0 REF

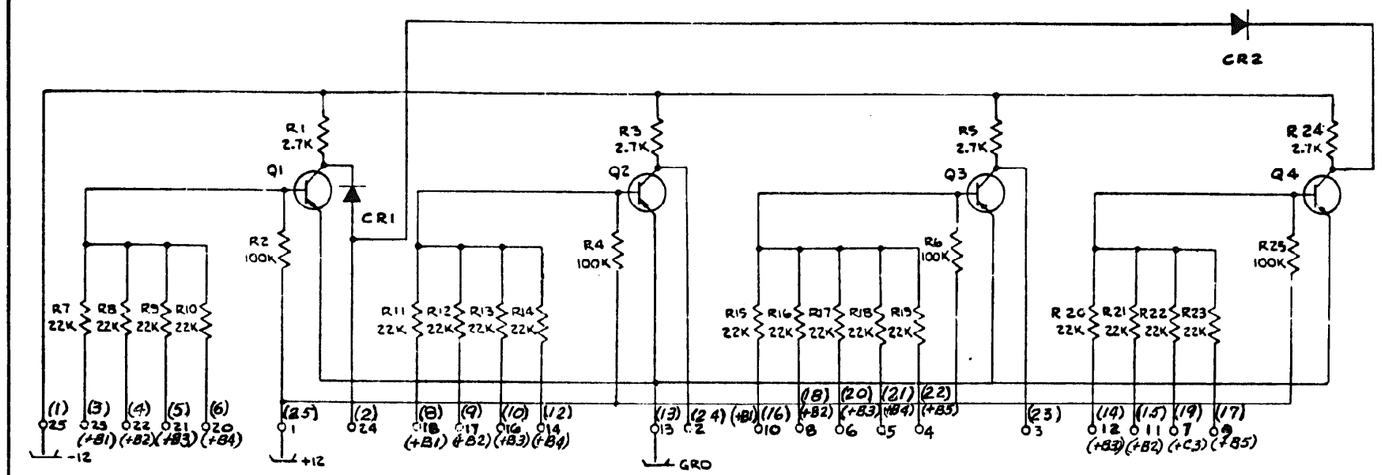
NOTE:

1. * DENOTES INVERTED SIGNAL.

GOVT APPD. JN 7-8-71

TEST LEGEND AS APPLICABLE,

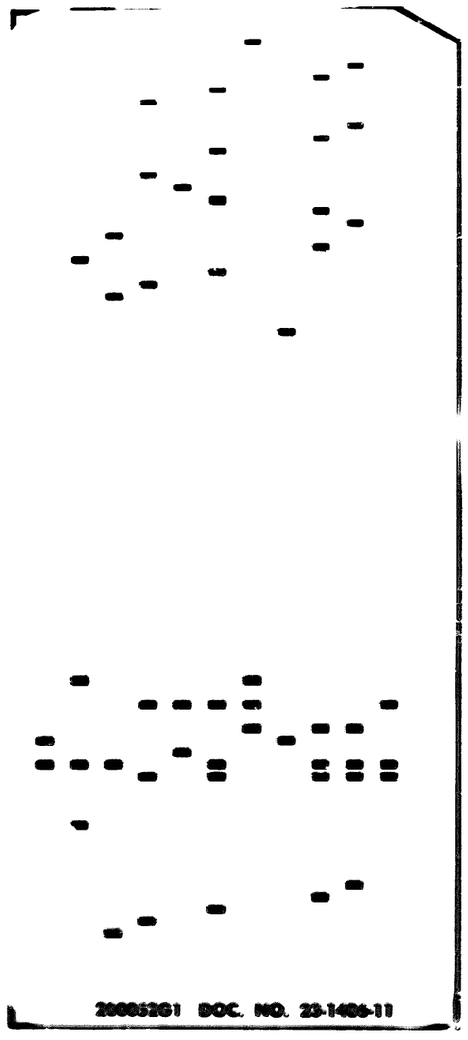
1. ICT--PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5 -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES



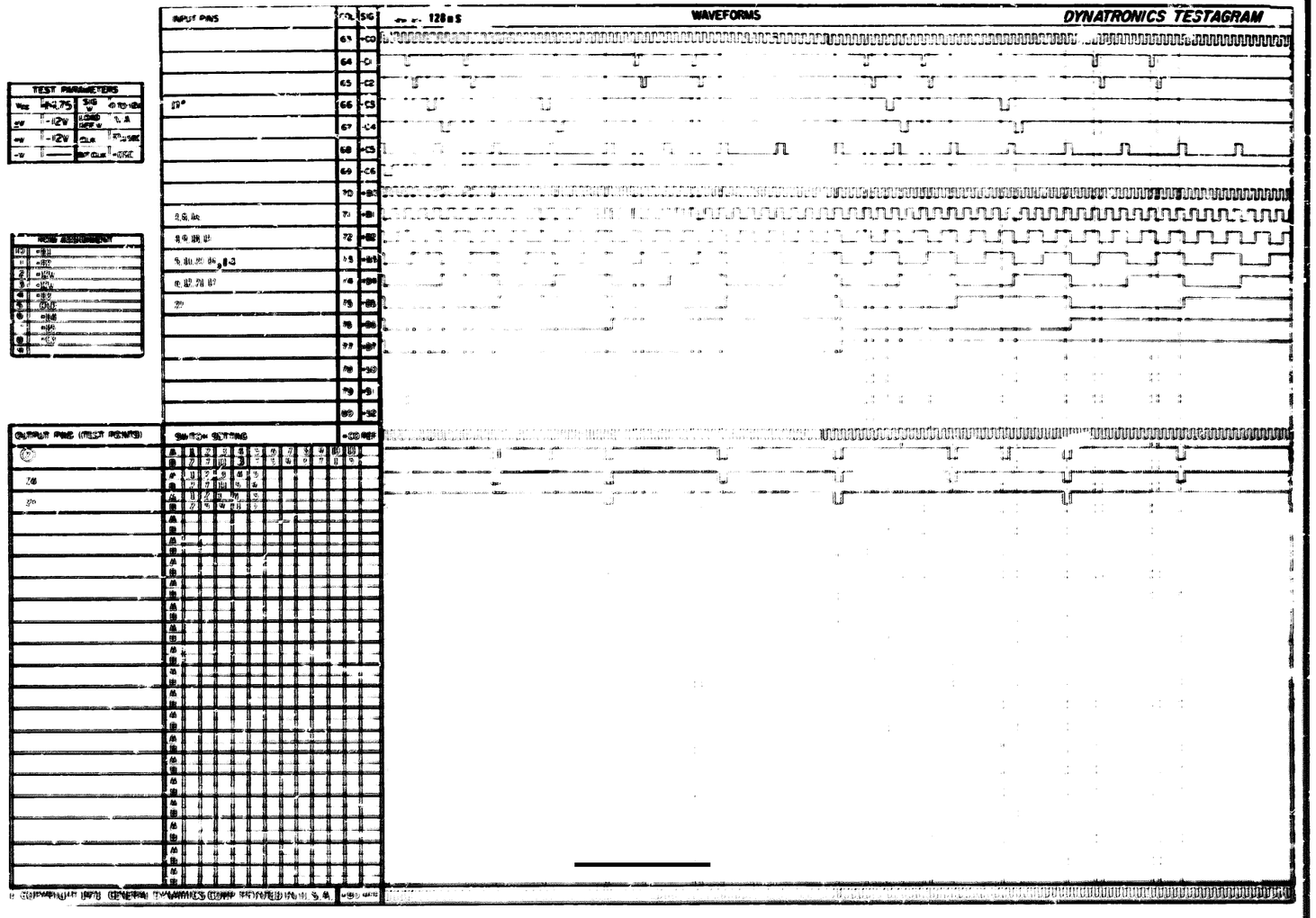
NOTES:
1. ALL RESISTANCE VALUES ARE IN OHMS ±5% ¼ WATT UNLESS OTHERWISE SPECIFIED.
2. REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION.

JN 7-8-71

P.C. Assembly 200052 G1

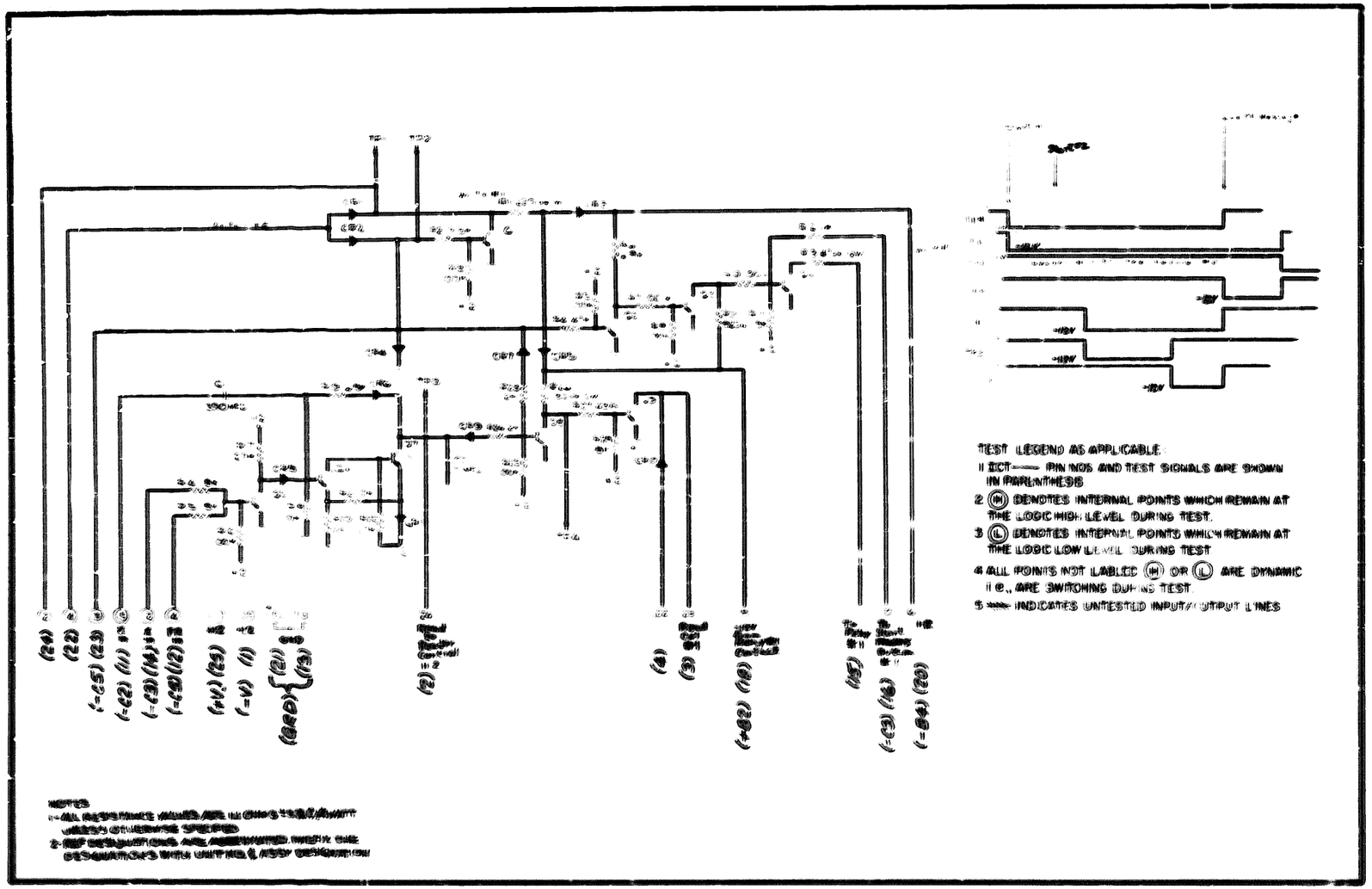


2000262 DOC. NO. 23-1406-11



NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.



TEST LEGEND AS APPLICABLE

1 ICT—— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST

4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.E., ARE SWITCHING DURING TEST

5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES

NOTES

1-ALL RESISTANCE VALUES ARE IN OHMS 1/8W/5% UNLESS OTHERWISE SPECIFIED

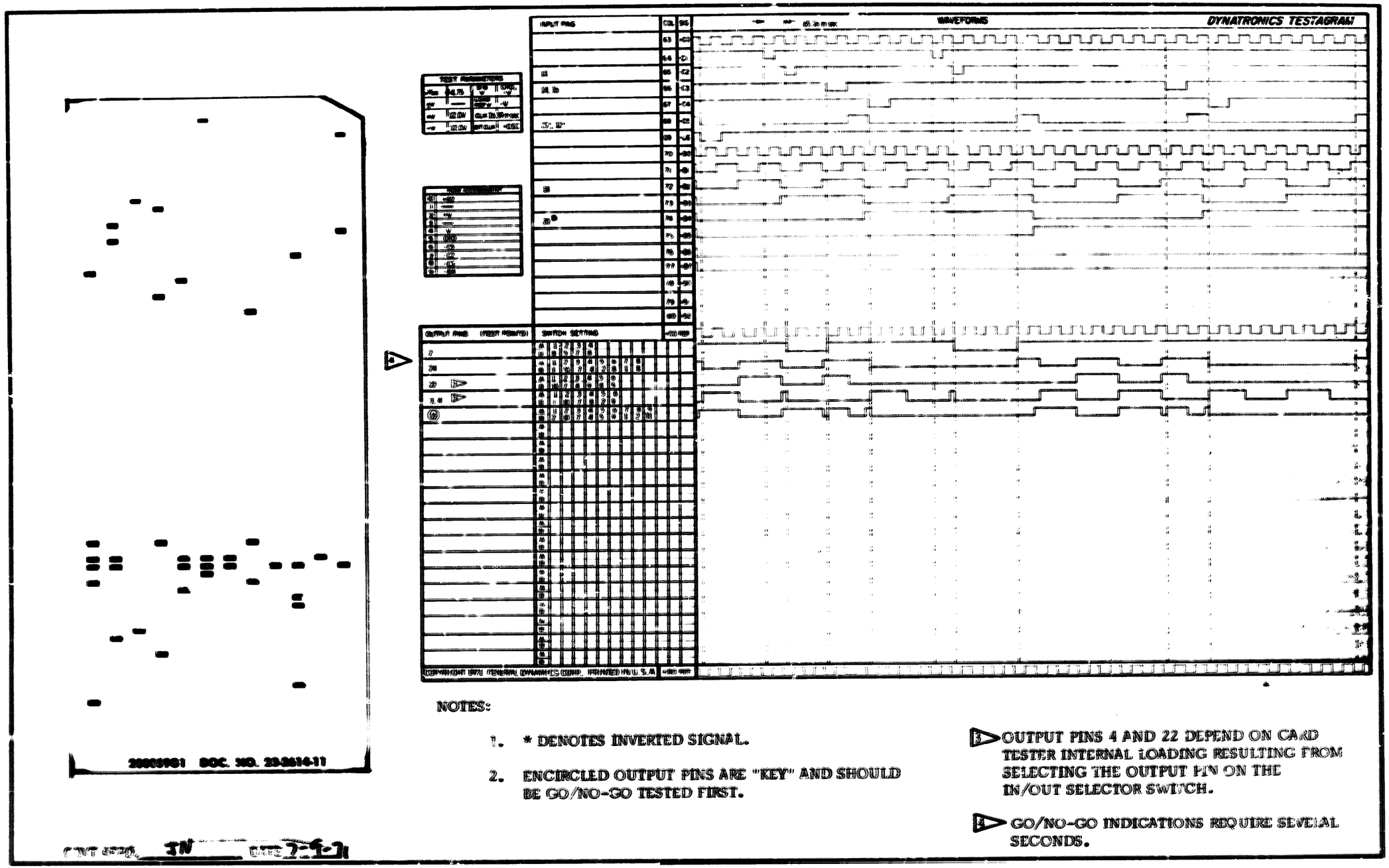
2-REF DESIGNATIONS ARE ABBREVIATED WITH THE DESIGNATORS WITH UNIT NO. & ASSY DESIGNATION

GOVT APPD. JSO DATE 7-9-71

P.C. Assembly 200059G1

P.C. Logic NAVSHIPS 0967 216 3010 Doc. No. 23- 2614-11

Fig. 5-30

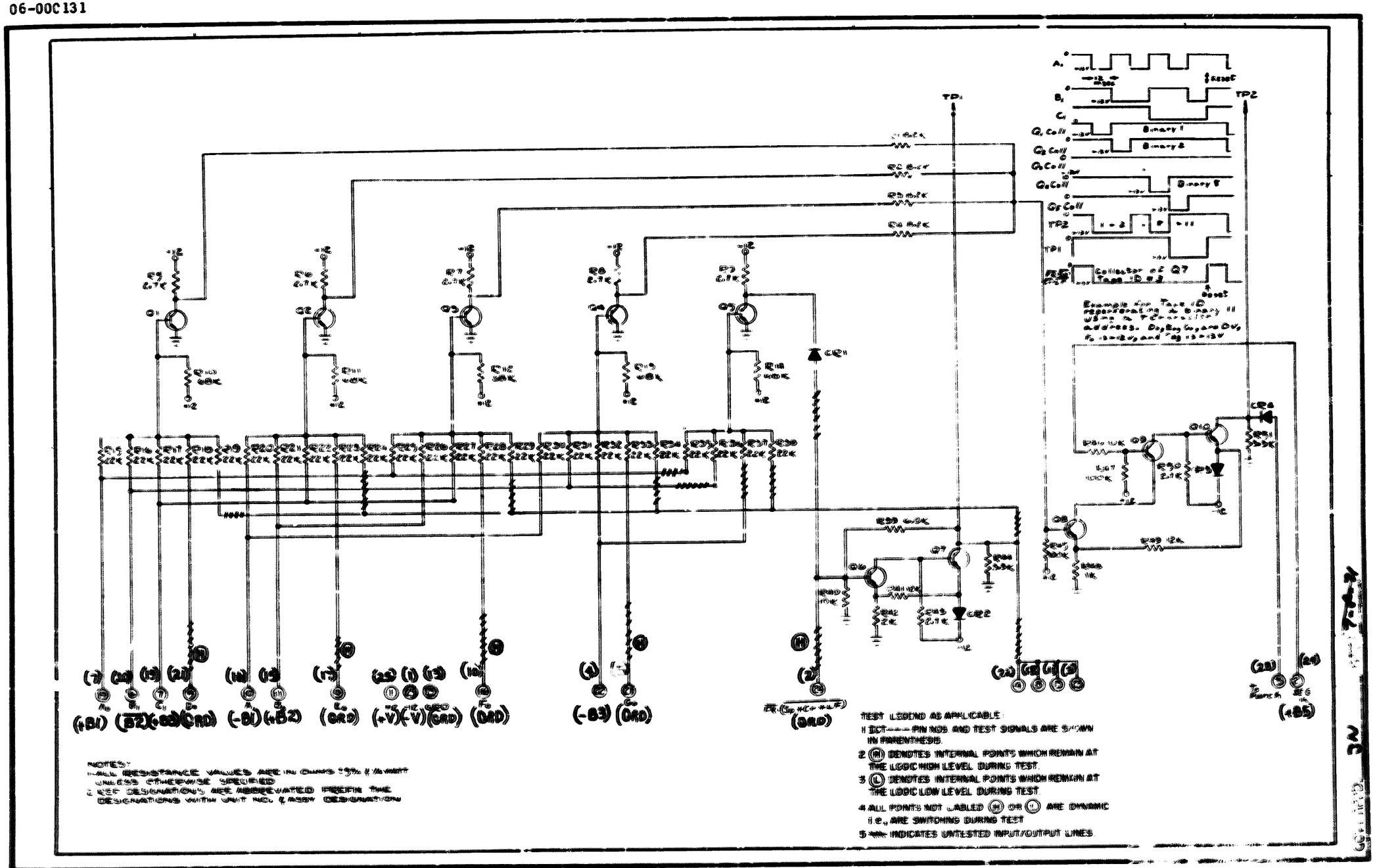


NOTES:

1. * DENOTES INVERTED SIGNAL.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

3 ▷ OUTPUT PINS 4 AND 22 DEPEND ON CARD TESTER INTERNAL LOADING RESULTING FROM SELECTING THE OUTPUT PIN ON THE IN/OUT SELECTOR SWITCH.

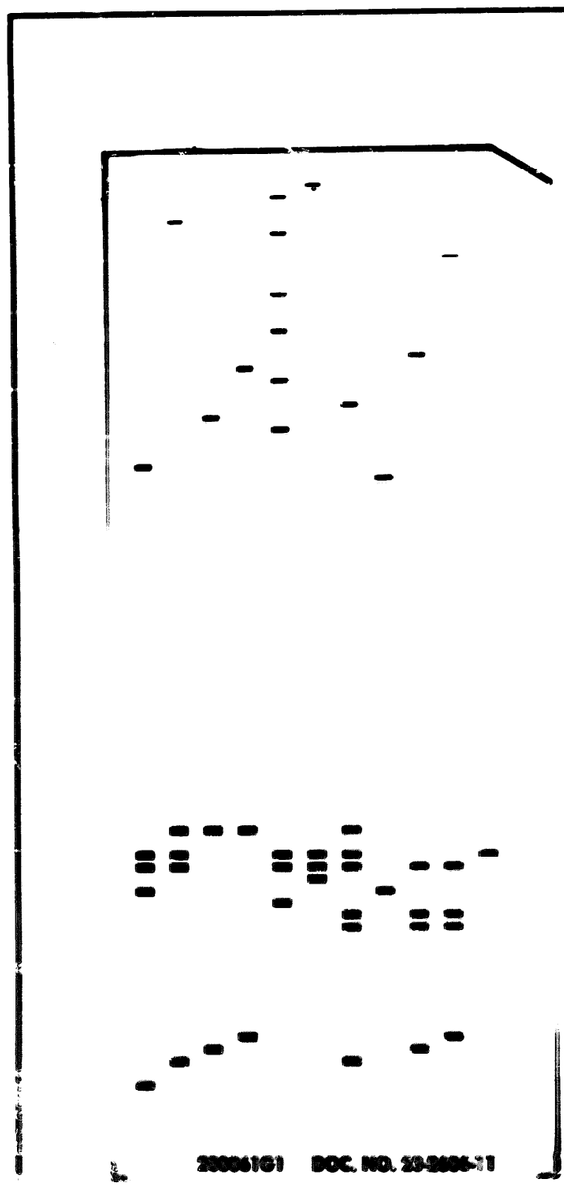
4 ▷ GO/NO-GO INDICATIONS REQUIRE SEVERAL SECONDS.

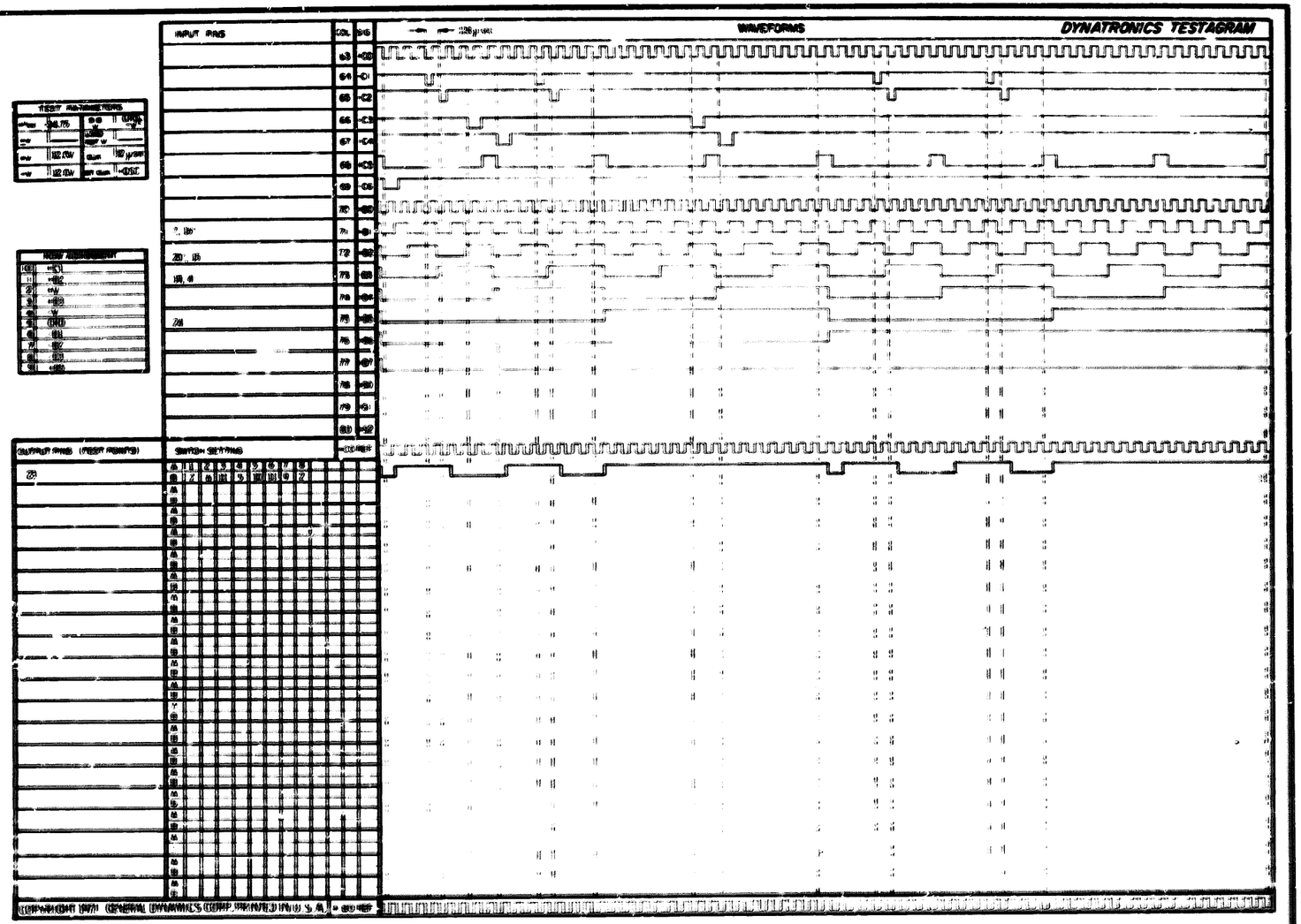


P.C. Assembly 200061G1

P.C. Logic NAVSHIPS 0967 216 0310 Doc. No. 23- 2606-11

Fig. 5-22





NOTE:

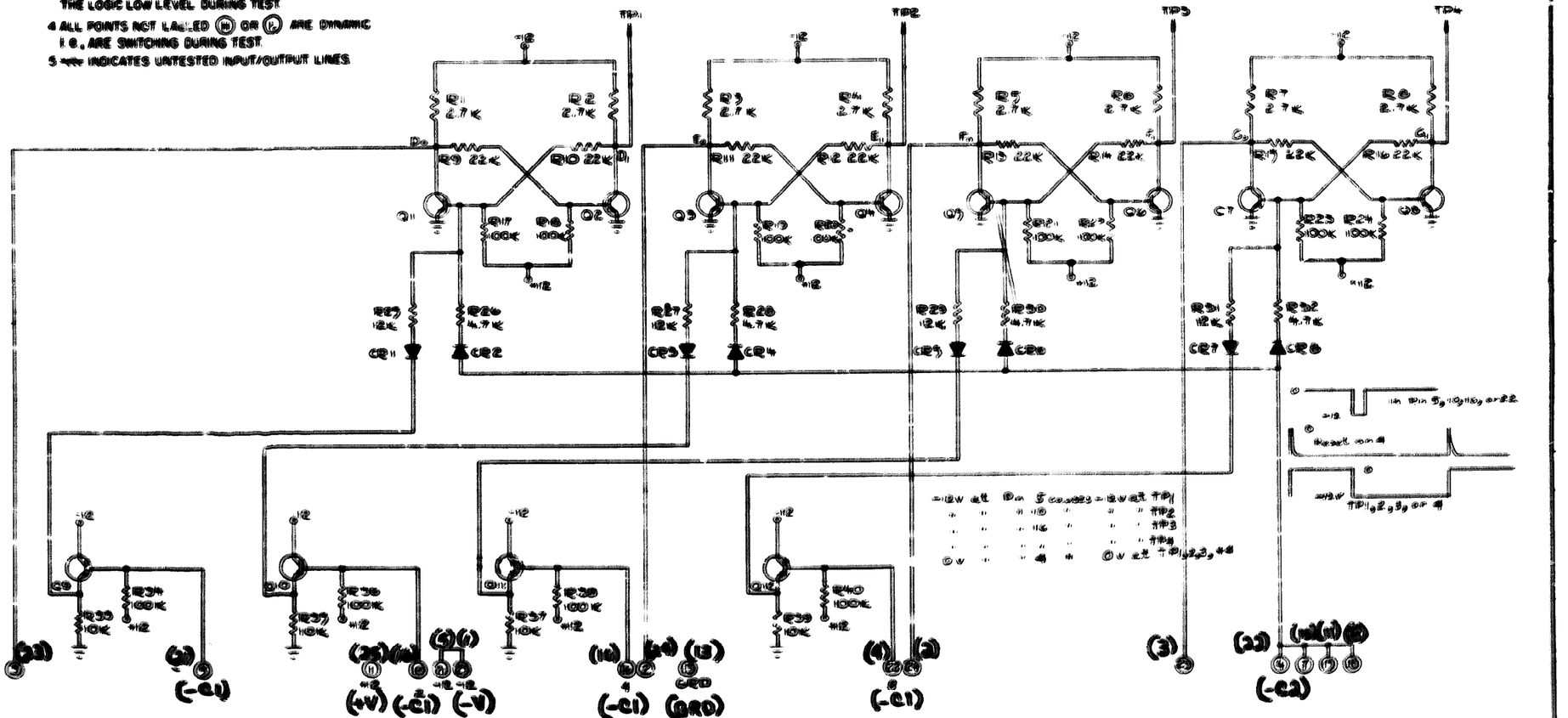
1. * DENOTES INVERTED SIGNAL.

2000161 DOC. NO. 23-2606-11

JN 7-8-71

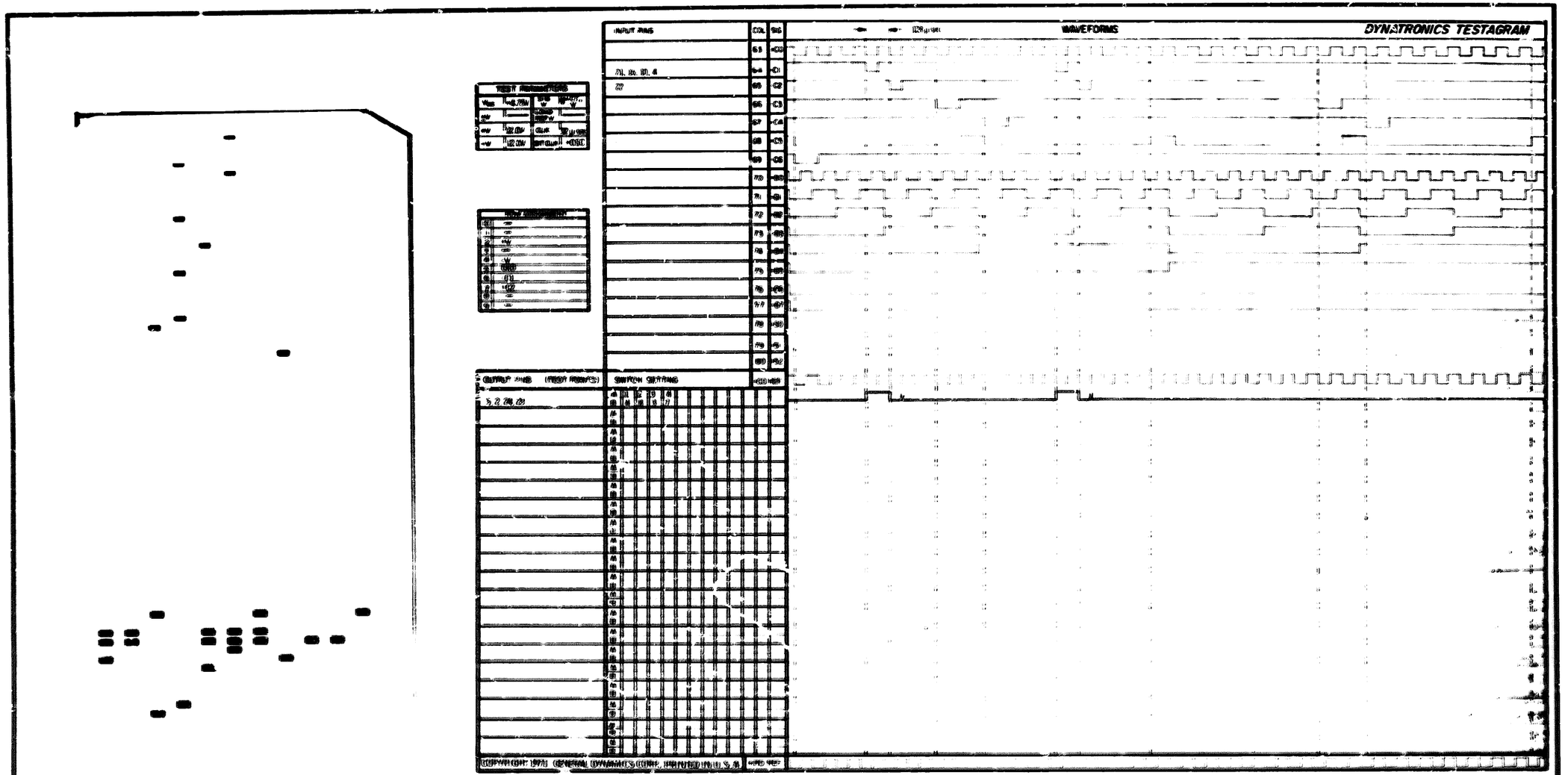
TEST LEGEND AS APPLICABLE:

1 ICT——— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC I.E., ARE SWITCHING DURING TEST.
5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES.



NOTES:
1-ALL RESISTANCE VALUES ARE IN OHMS ±5% 1/4 WATT UNLESS OTHERWISE SPECIFIED
2-REF DESIGNATIONS ARE ABBREVIATED. PREFIX WITH DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION

P.C. Assembly 200063G1
P.C. Logic NAVSHIPS 0967 216 3010 Doc. No. 23-2607-11
Fig. 5-23



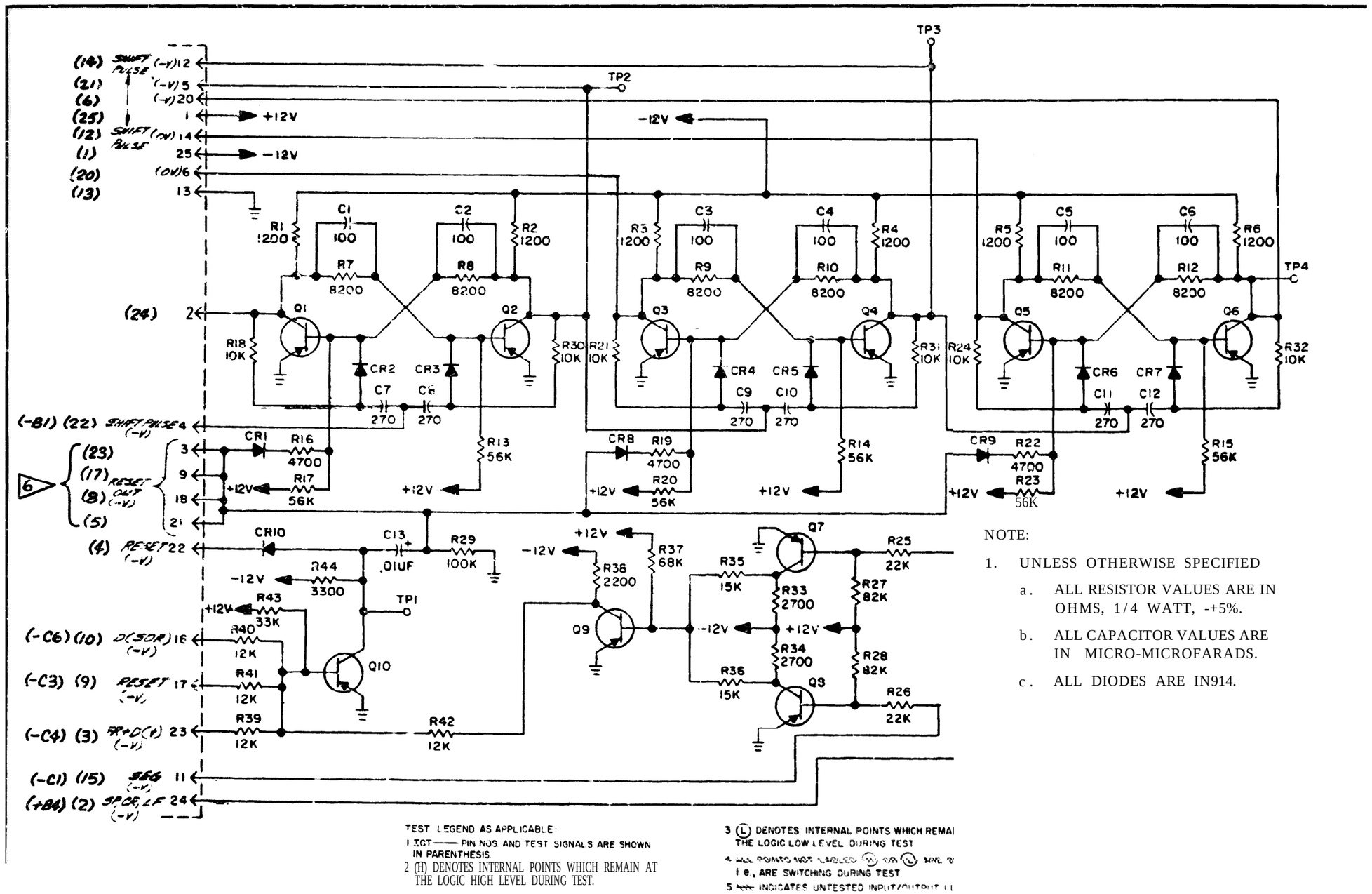
NOTE:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

29006361 DOC. NO. 23-2607-11

Doc. No. 23- 2607-11

P.C. Assembly 200063G1
P.C. Logic NAVSHIPS 0967 216 3010
Fig. 5-23



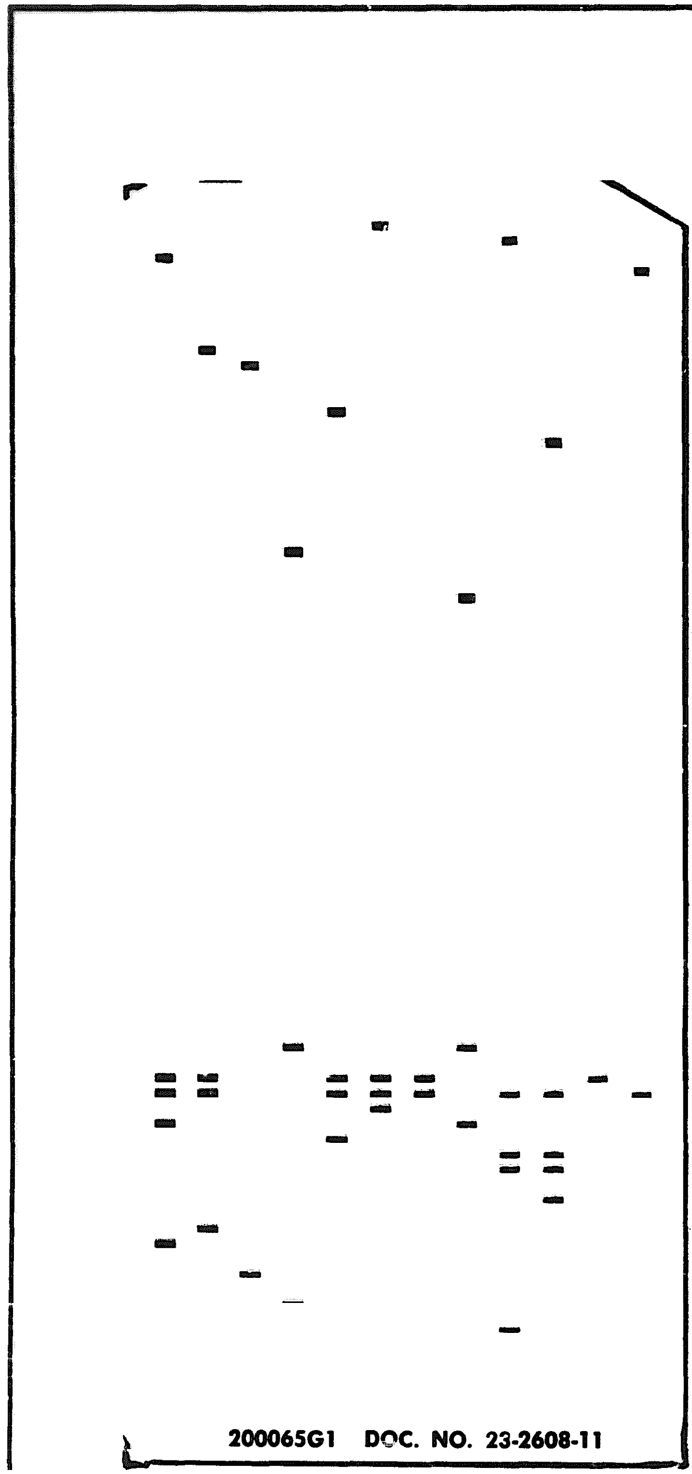
NOTE:

1. UNLESS OTHERWISE SPECIFIED
   a. ALL RESISTOR VALUES ARE IN OHMS, 1/4 WATT, -+5%.
   b. ALL CAPACITOR VALUES ARE IN MICRO-MICROFARADS.
   c. ALL DIODES ARE IN914.

TEST LEGEND AS APPLICABLE:
1 ICT —— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAI THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABELED (H) OR (L) ARE i e., ARE SWITCHING DURING TEST
5 XXX INDICATES UNTESTED INPUT/OUTPUT

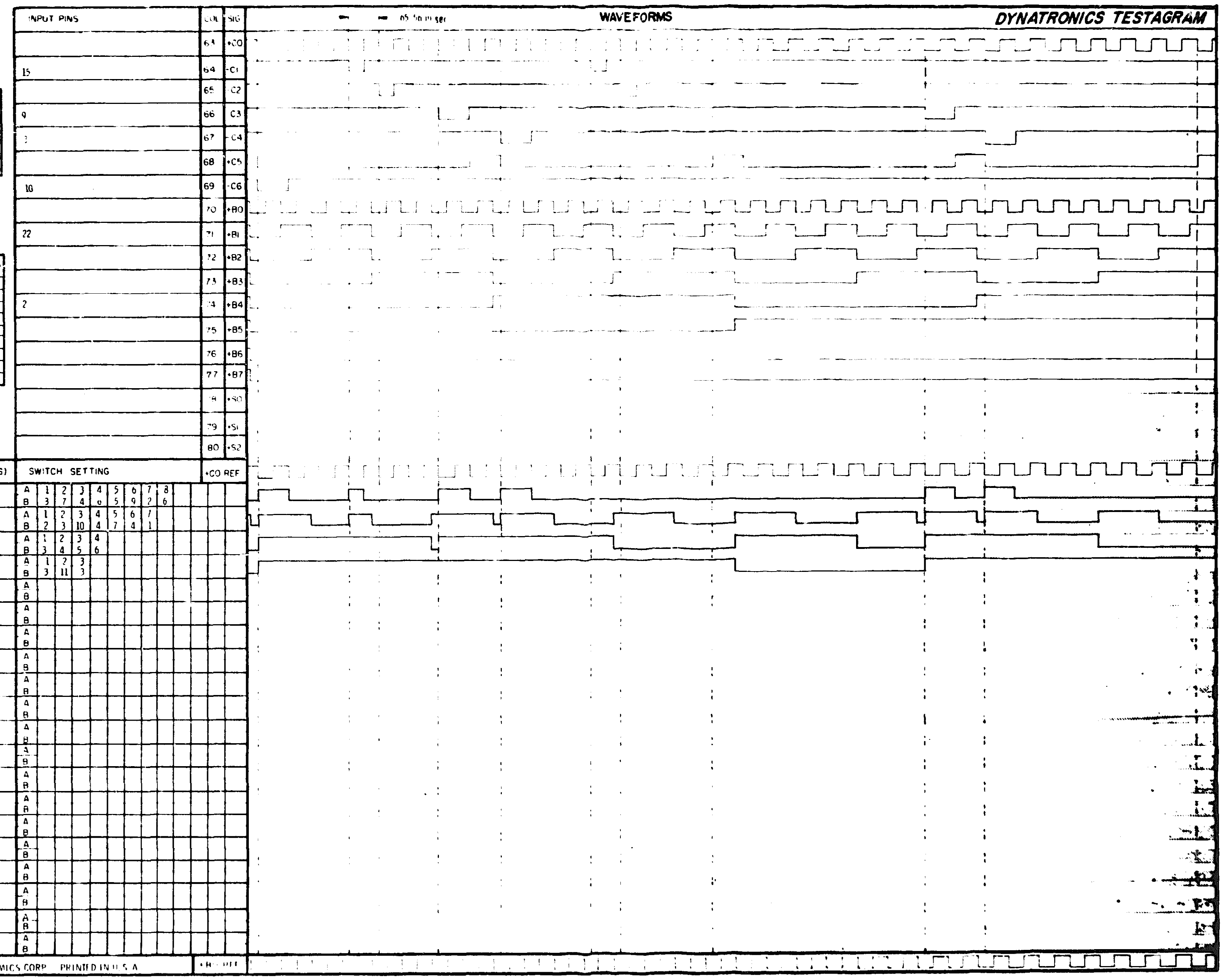
P.C. Assembly 200065G1
P.C. Logic NAVSHIPS 0967 216 3010

Fig. 5-40



TEST PARAMETERS			
Vcc	+4.75V	SIG V	GRD, -V
±V	—	LOAD REF V	-V
+V	12.0V	CLK	16.39MS
-V	12.0V	BIT CLK	+OSC

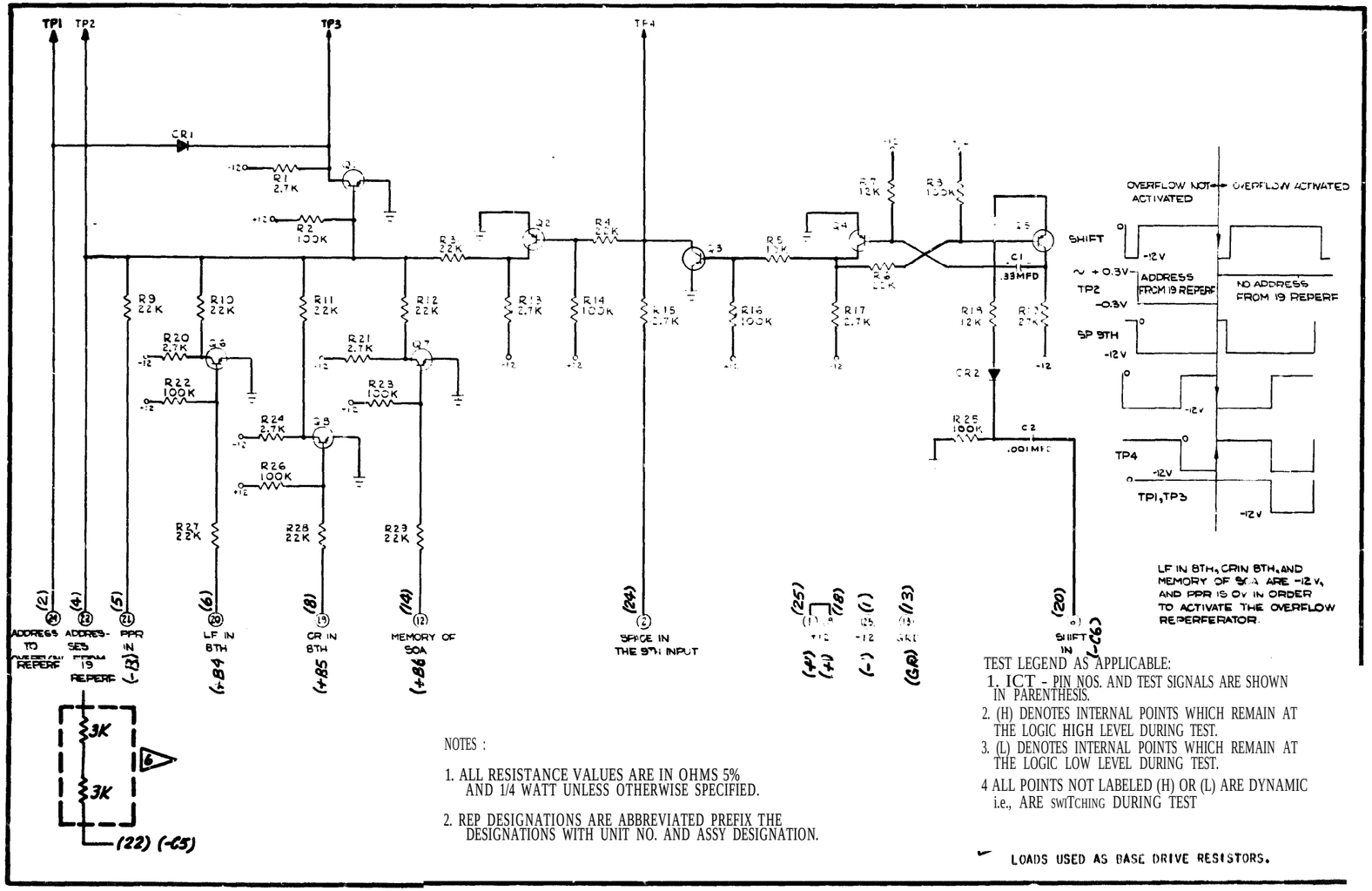
ROW ASSIGNMENT	
10	-C1
1	+B4
2	+V
3	—
4	-V
5	GRD
6	-B1
7	-C6
8	-C3
9	-C4



NOTES:

1. *DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. WAIT SEVERAL SECONDS FOR GO/NO-GO INDICATION.

GOVT APPD. ꟷ JN DATE 8-19-71



NOTES :

1. ALL RESISTANCE VALUES ARE IN OHMS 5% AND 1/4 WATT UNLESS OTHERWISE SPECIFIED.
2. REP DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION.

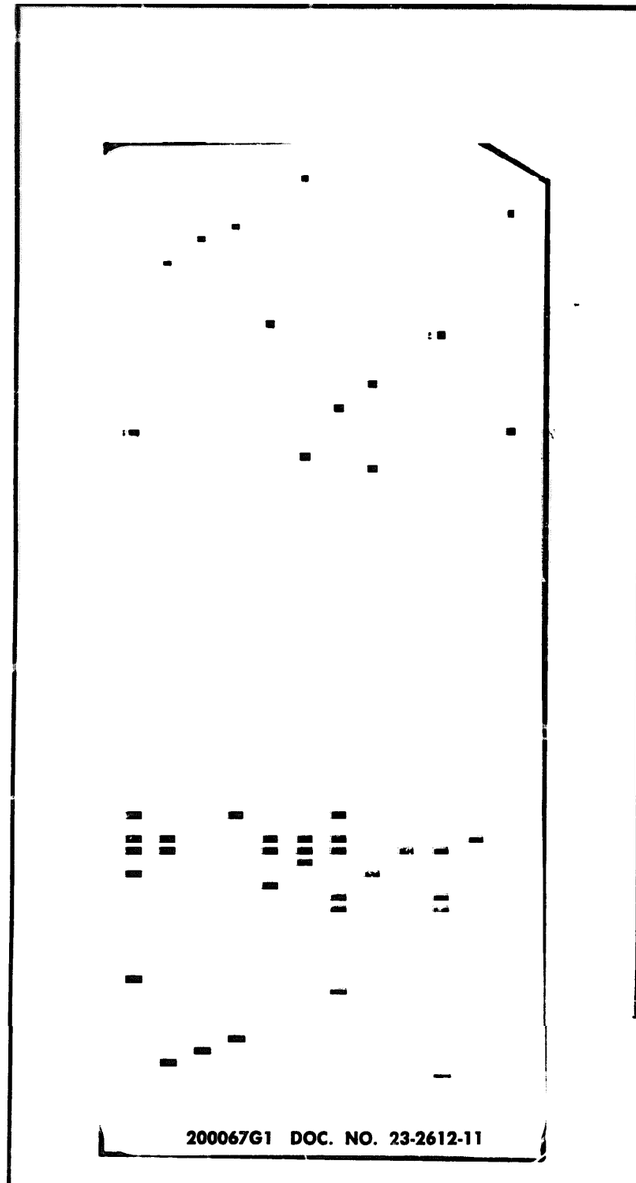
TEST LEGEND AS APPLICABLE:

1. ICT - PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST

LOADS USED AS BASE DRIVE RESISTORS.

JN

P.C. Assembly 200067G1
P.C. Logic NAVSHIPS 0967 216 3020 Doc. No. 23- 2612-11
Fig, 5-28



200067G1 DOC. NO. 23-2612-11

GOVT APPD. JN DATE 7-8-71

TEST PARAMETERS

+Vcc	+4.75	SIG V	GRD -V
±V	—	LOAD REF V	—
+V	12.0V	CLK	1.2 µsec
-V	12.0V	BIT CLK	÷OSC

ROW ASSIGNMENT

10	+B6
1	—
2	+V
3	-C6
4	-V
5	GRD
6	-B3
7	+B4
8	+B5
9	-C5

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
22	68	+C5
20	69	-C6
	70	+B0
	71	+B1
	72	+B2
5*	73	+B3
6	74	+B4
8	75	+B5
14	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
SWITCH SETTING		+C0 REF

OUTPUT PINS (TEST POINTS)

2

TP 4 (REF ONLY)

SWITCH SETTING: A 1 2 3 / B 6 10 # / A - / B

+B0 REF

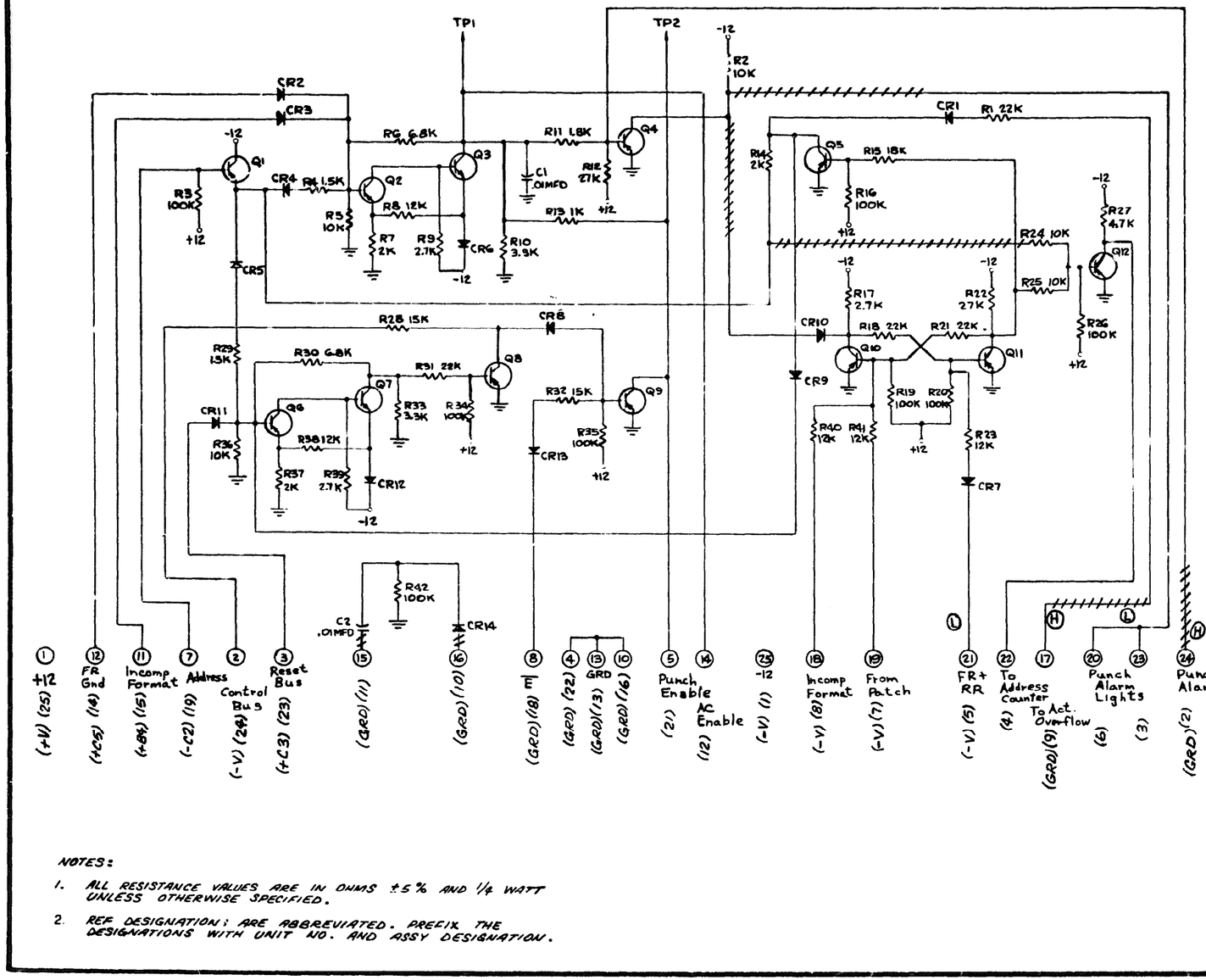
WAVEFORMS — 128 µ sec — APPROXIMATELY 3 m sec

DYNATRONICS TESTAGRAM

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST-IS GO INDICATION.



NOTES:

1. ALL RESISTANCE VALUES ARE IN OHMS ±5% AND 1/4 WATT UNLESS OTHERWISE SPECIFIED.
2. REF DESIGNATION; ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION.

TEST LEGEND AS APPLICABLE:

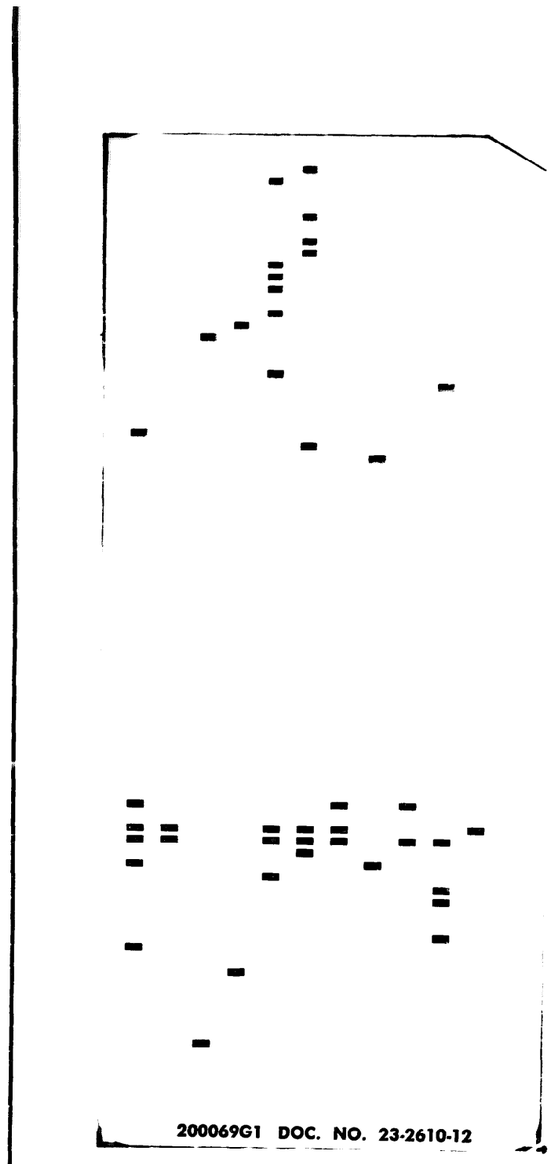
1. ICT- PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e.. ARE SWITCHING DURING TEST.
5. -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES.

7-8-71

JW

P.C. Assembly 200069G1

P.C. Logic NAVSHIPS 0967 216 3010 Doc. No. 23- 2610-12
Fig. 5-26



TEST PARAMETERS			
$+V_{cc}$	+4.75	SIG X	GRD. -V
±V		LOAD REF V	
+V	12.0V	CLK	32 μ sec
-V	12.0V	INT CLK	+OSC

ROW ASSIGNMENT	
10	-C2
1	—
2	+V
3	—
4	-V
5	GRD
6	+C5
7	+B4
8	—
9	+C3

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
19	65	-C2
23*	66	-C3
	67	-C4
14	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
15	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
OUTPUT PINS (TEST POINTS)	SWITCH SETTING	+C0 REF
21	A 1 2 3 4 / B 5 6 4 5	
12	A 1 2 3 4 / B 5 6 4 5	

WAVEFORMS — → ← 128 μ sec

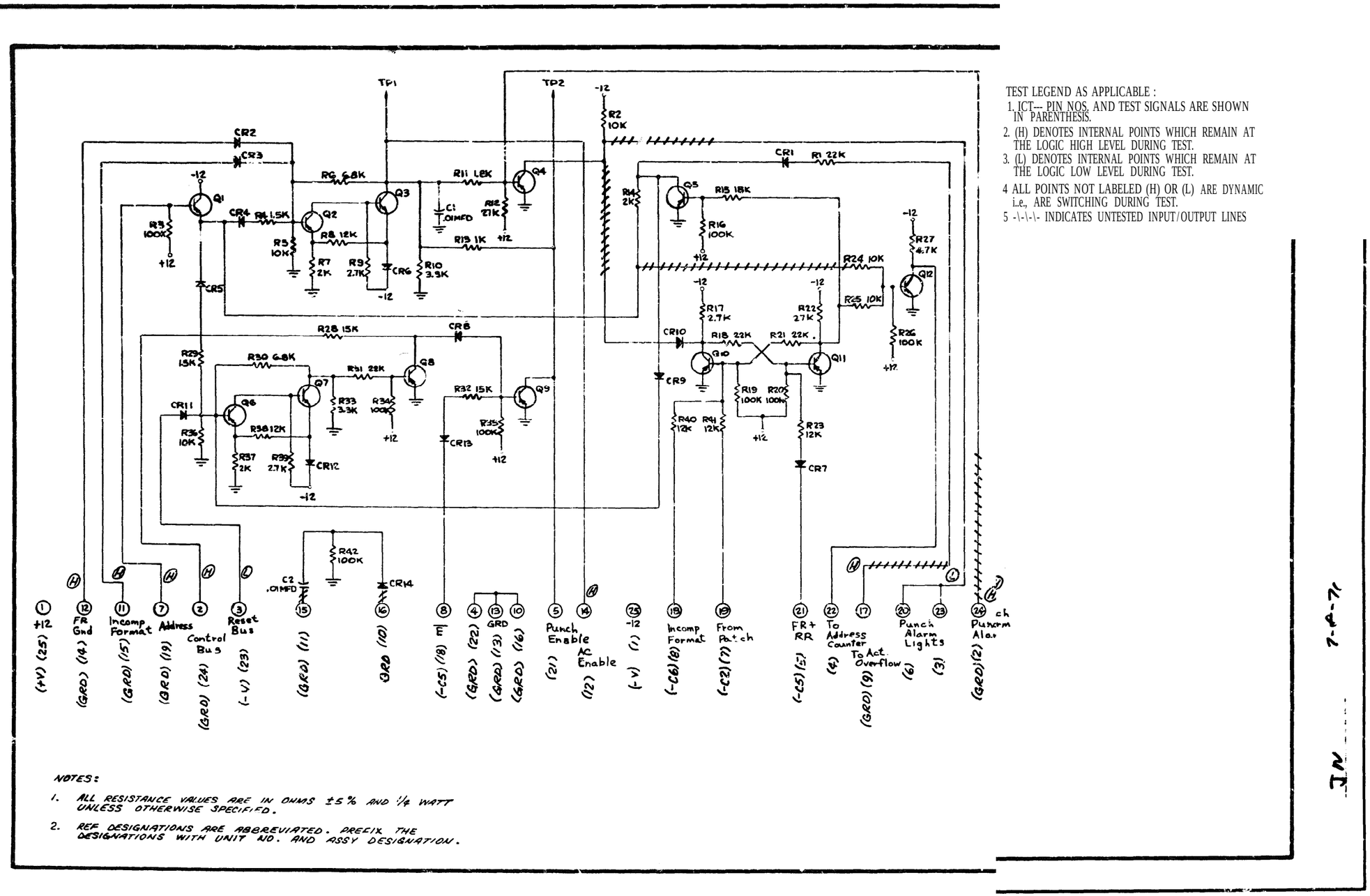
DYNATRONICS TESTAGRAM

NOTE:

1. * DENOTES INVERTED SIGNAL.

200069G1 DOC. NO. 23-2610-12

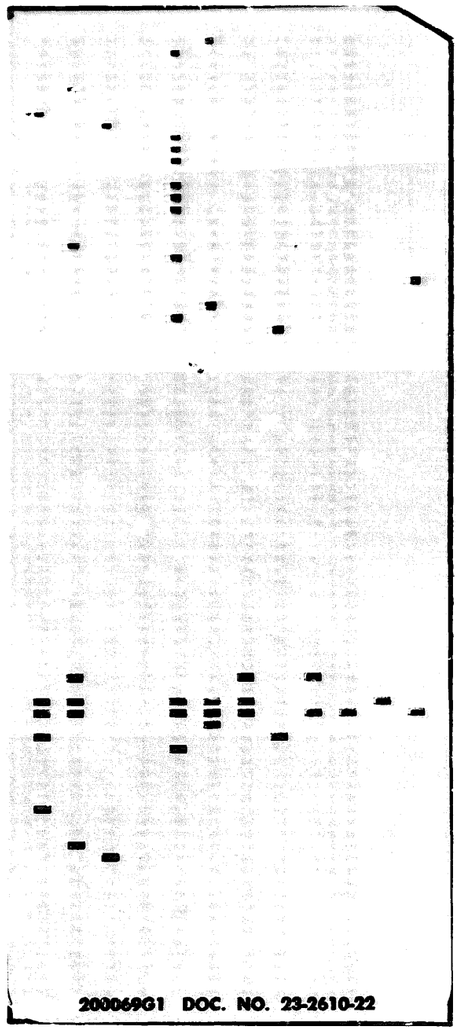
CCVT APPD. JN DATE 7-8-71



P.C. Assembly 200069G1

P.C. Logic NAVSHIPS 0967 216 3310 Doc. NO. 23-2610-22

Fig. 5-26



TEST PARAMETERS			
+Vcc	+4.75	STB V	GRD -V
5V	——	LOAD REF V	-V
+V	+2.0V	CLR	32 µs SEC
-V	-2.0V	BIT CLR	+05C

ROW ASSIGNMENT	
10	—
1	—
2	+V
3	—
4	-V
5	GRD
6	—
7	-C0
8	-C5
9	-C7

INPUT PINS

	COL	SIG
	63	+C0
	64	-C1
7	65	-C2
	66	-C3
	67	-C4
9, 28	68	+C5
8	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS) — SWITCH SETTING — +C0 REF

4	A	1	2	3	4
	B	3	9	7	8
21	A	1	2	3	4
	B	3	9	2	6

WAVEFORMS — 178 µ SEC — DYNATRONICS TESTAGRAM

 +B0 REF

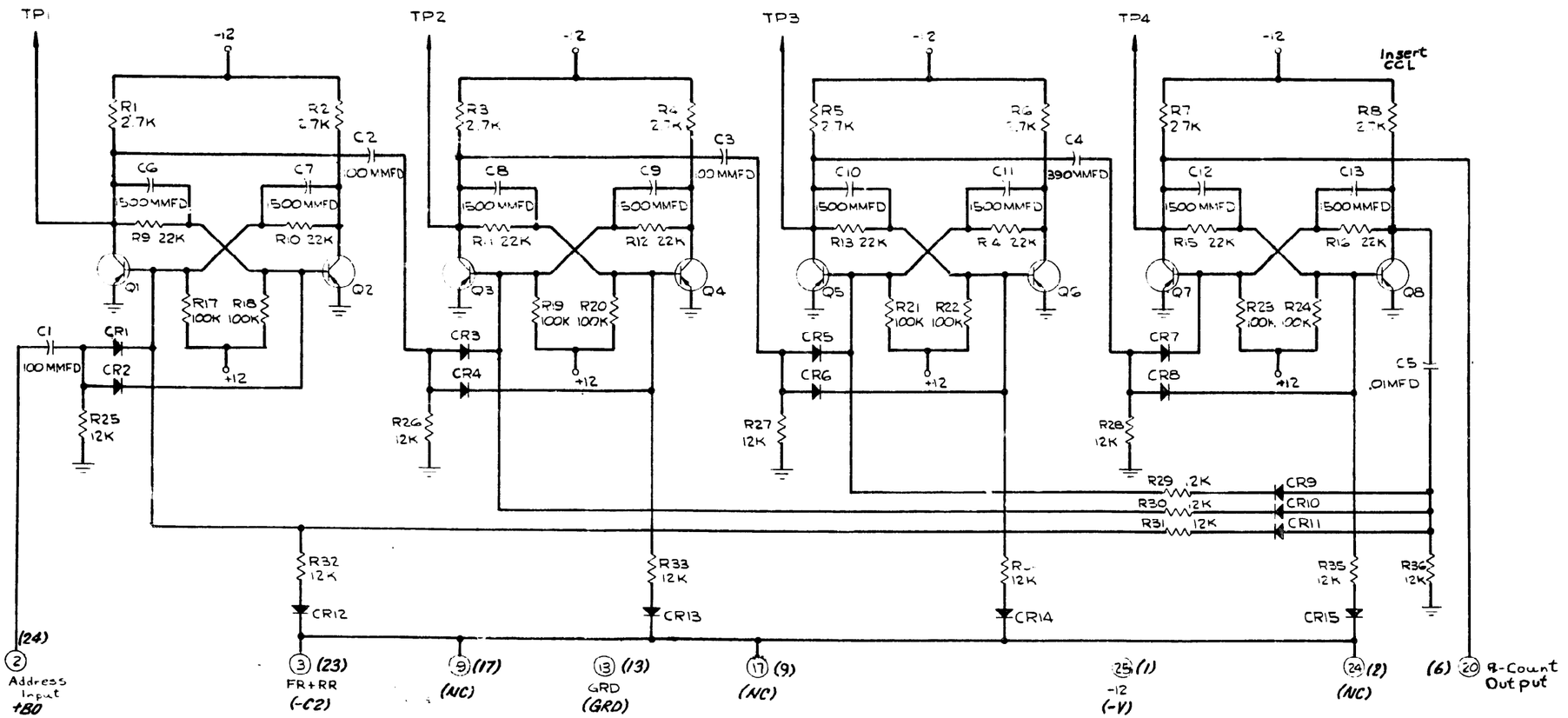
NOTES:

1. * DENOTES INVERTED SIGNAL.

GOVT APPD. JN DATE 7-8-71

TEST LEGEND AS APPLICABLE:

1. ICT- PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES.

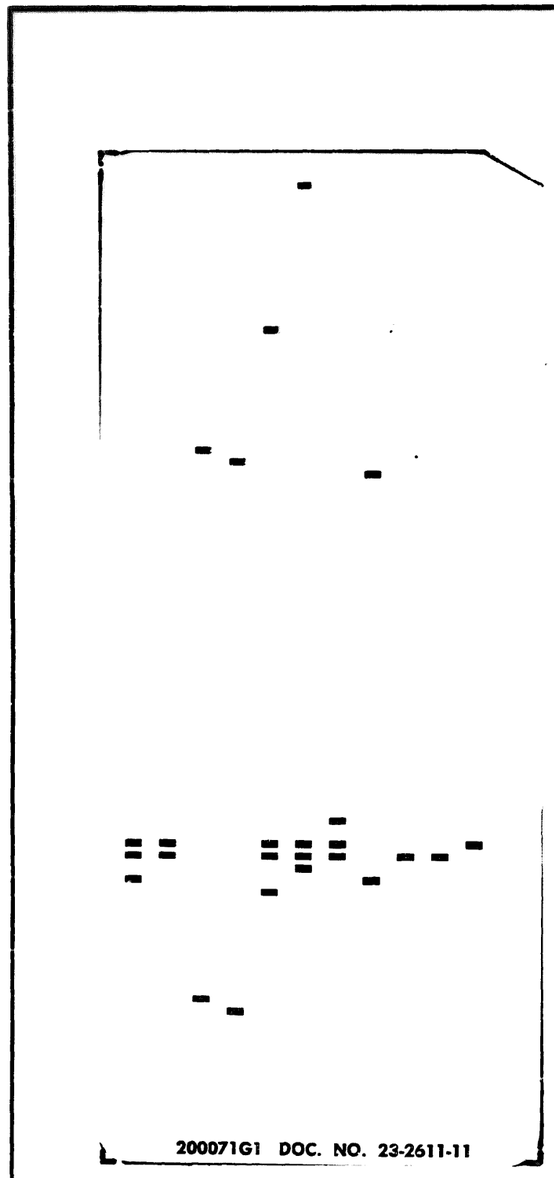


NOTES:

1- ALL RESISTANCE VALUES ARE IN OHMS ±5% & 1/4 WATT UNLESS OTHERWISE SPECIFIED

2- REF DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION

APPD. _____ DATE _____



TEST PARAMETERS

V_{CC}	+4.75	STB V	GND -V
+V	—	LOAD REF V	—
+V	12.0V	CLK	30μSEC
-V	12.0V	BIT CLK	+05C

ROW ASSIGNMENT

10	—
1	—
2	+V
3	—
4	-V
5	GRD
6	+B0
7	-C2
8	—
9	—

INPUT PINS

23

24

OUTPUT PINS (TEST POINTS)

6

SWITCH SETTING

	1	2	3	4
A	1	II	4	3
B				

COL SIG

63	+C0
64	-C1
65	-C2
66	-C3
67	-C4
68	+C5
69	-C6
70	+B0
71	+B1
72	+B2
73	+B3
74	+B4
75	+B5
76	+B6
77	+B7
78	+S0
79	+S1
80	+S2
	+C0 REF
	+B0 REF

WAVEFORMS

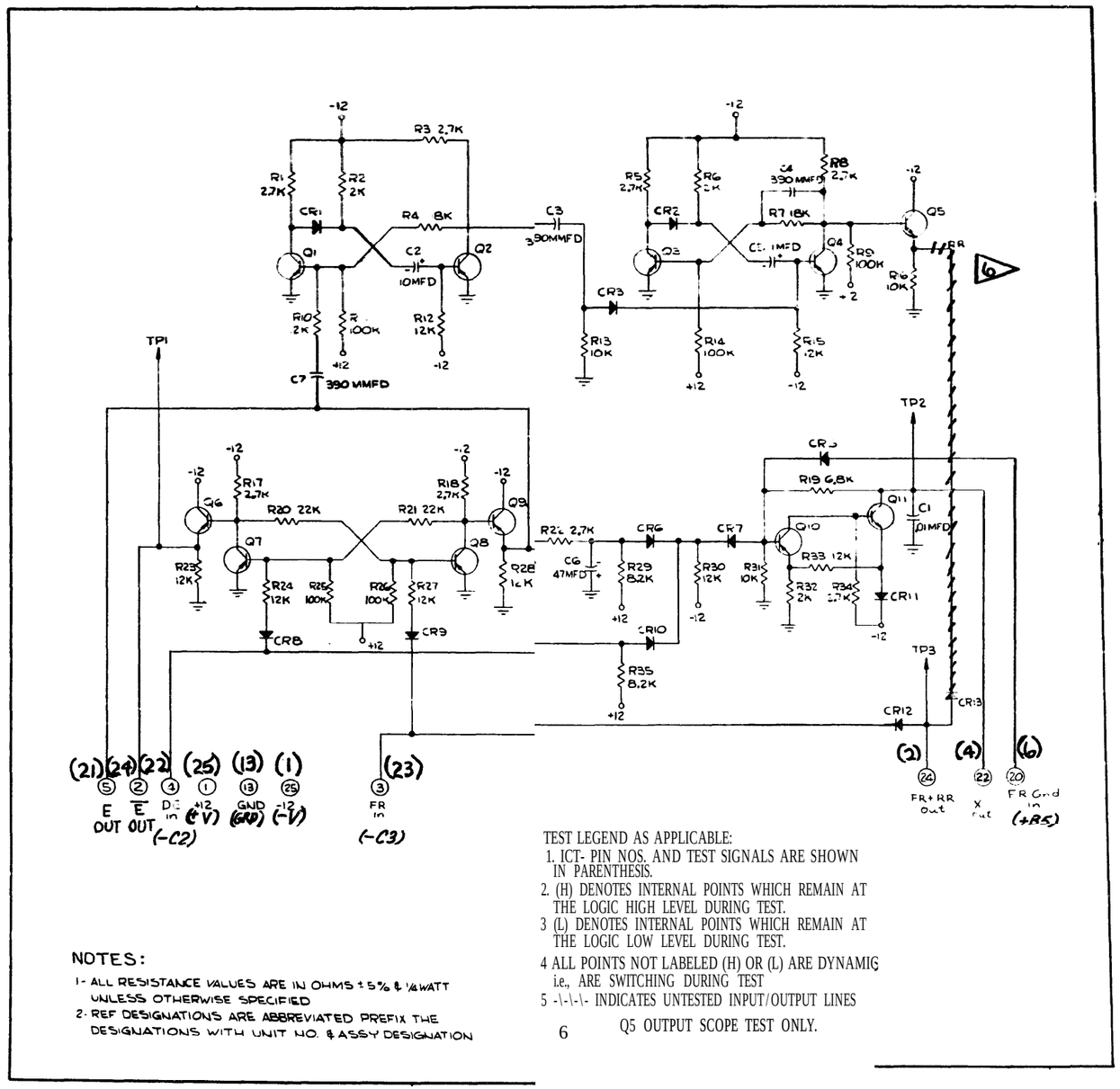
DYNATRONICS TESTAGRAM

NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

200071G1 DOC. NO. 23-2611-11

GOVT APPD. _____ DATE 8-13-71



NOTES:

1- ALL RESISTANCE VALUES ARE IN OHMS ± 5% & ¼WATT UNLESS OTHERWISE SPECIFIED
2- REF DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION

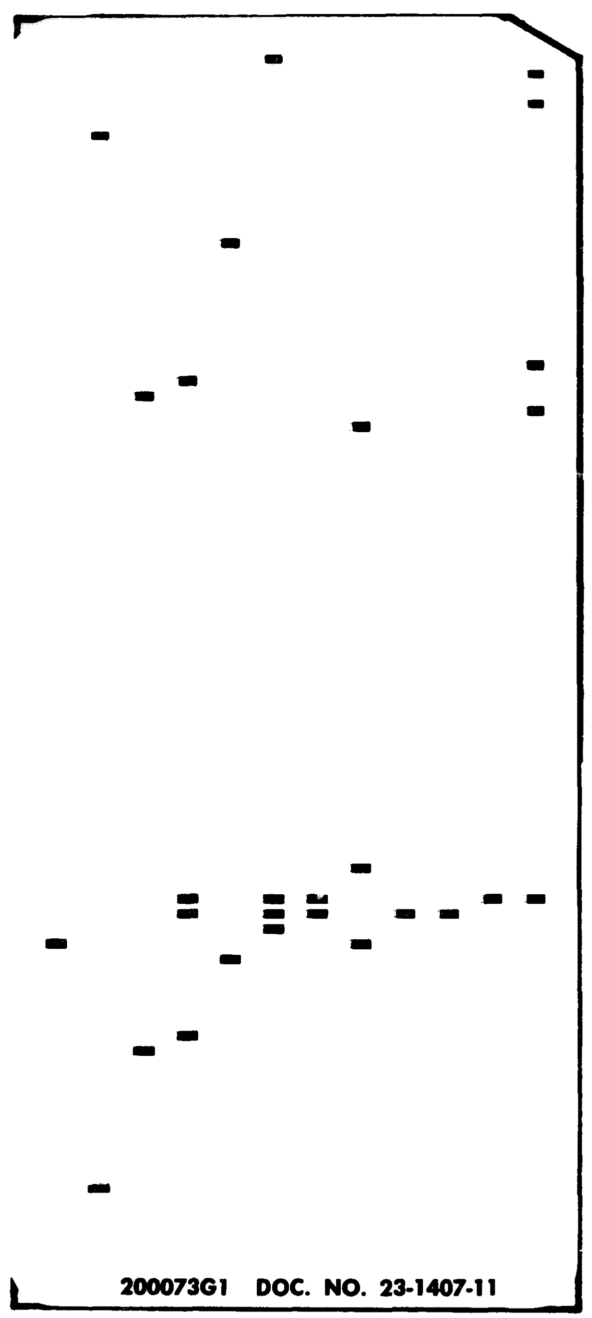
TEST LEGEND AS APPLICABLE:

1. ICT- PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST
5 -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES
6 Q5 OUTPUT SCOPE TEST ONLY.

JN DATE 7-8-7

P.C. Assembly 200073/G1

P.C. Logic Navships 09672163010 Doc. No. 23- 1407-11
Fig. 5-15



GOVT APPD. JN DATE 7-9-71

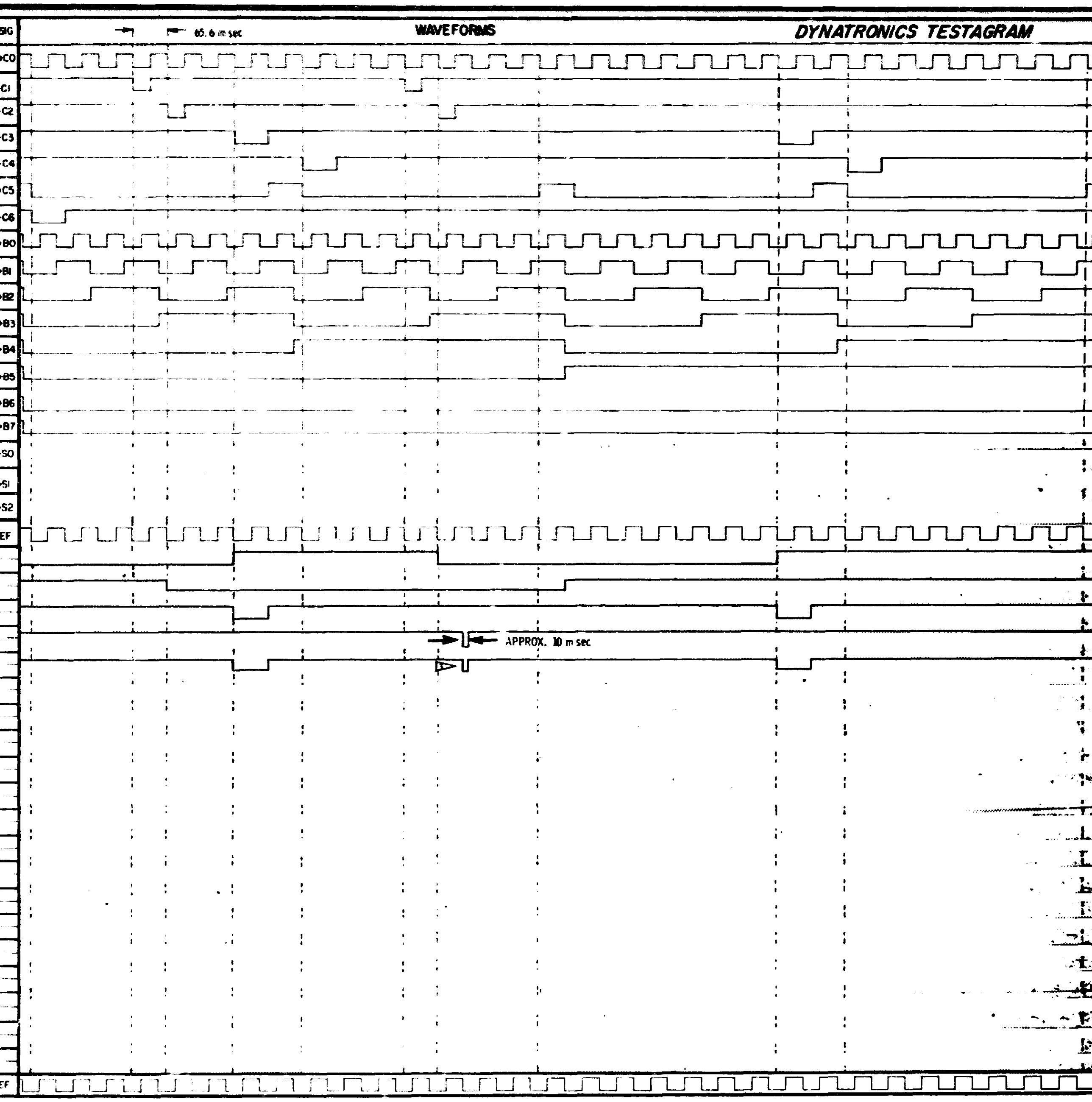
DYNATRONICS TESTAGRAM

TEST PARAMETERS			
Vcc	+4.75	SIG V	GRD, -V
±V	—	LOAD REF V	12, GRD
+V	12	CLK	16.39 m sec
-V	12	BIT CLK	+OSC

ROW ASSIGNMENT	
0	—
1	—
2	+12V
3	—
4	-12V
5	GRD
6	-C2
7	-C3
8	+B5
9	—

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
22	65	-C2
23	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
6	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2

OUTPUT PINS (TEST POINTS)	SWITCH SETTING			
4▷ 21, 24*	A	1	2	3
	B	5	7	3
4	A	1	2	
	B	8	11	
2	A	1	2	
	B	5	9	
Q5 EMITTER (FOR REF. ONLY) 3▷	A			
	B			
T.P.3 SCOPE TEST ONLY	A			
	B			



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

3▷ THIS PULSE IS ASYNCHRONOUS WITH TESTER WAVEFORMS AND WILL OCCUR AT ANY POINT WITHIN THE FRAME.

4▷ GO/NO-GO INDICATIONS REQUIRE SEVERAL SECONDS.

TEST LEGEND AS APPLICABLE:

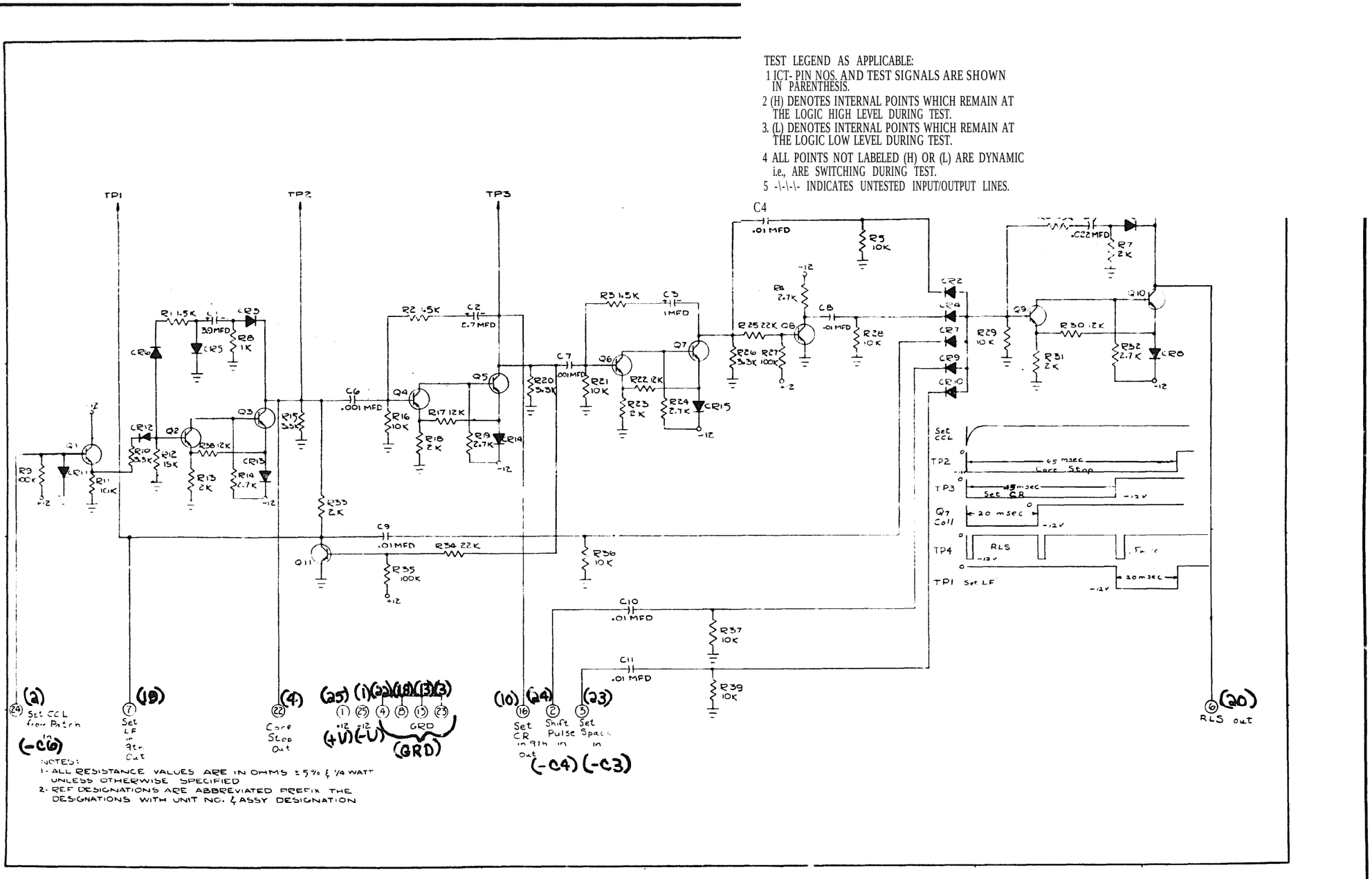
1 ICT- PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.

2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

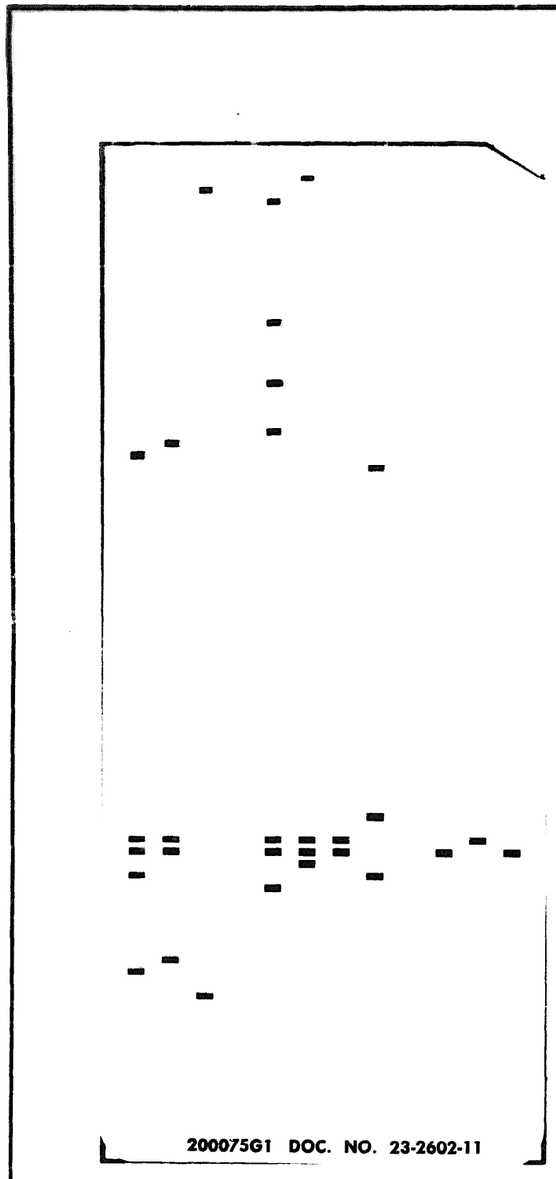
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.

4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.

5 -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES.



P.C. Assembly 200075G1
P.C. Logic NAVSHIPS 0967-216-3010 Doc. No. 23-2602-11
Fig. 5-16



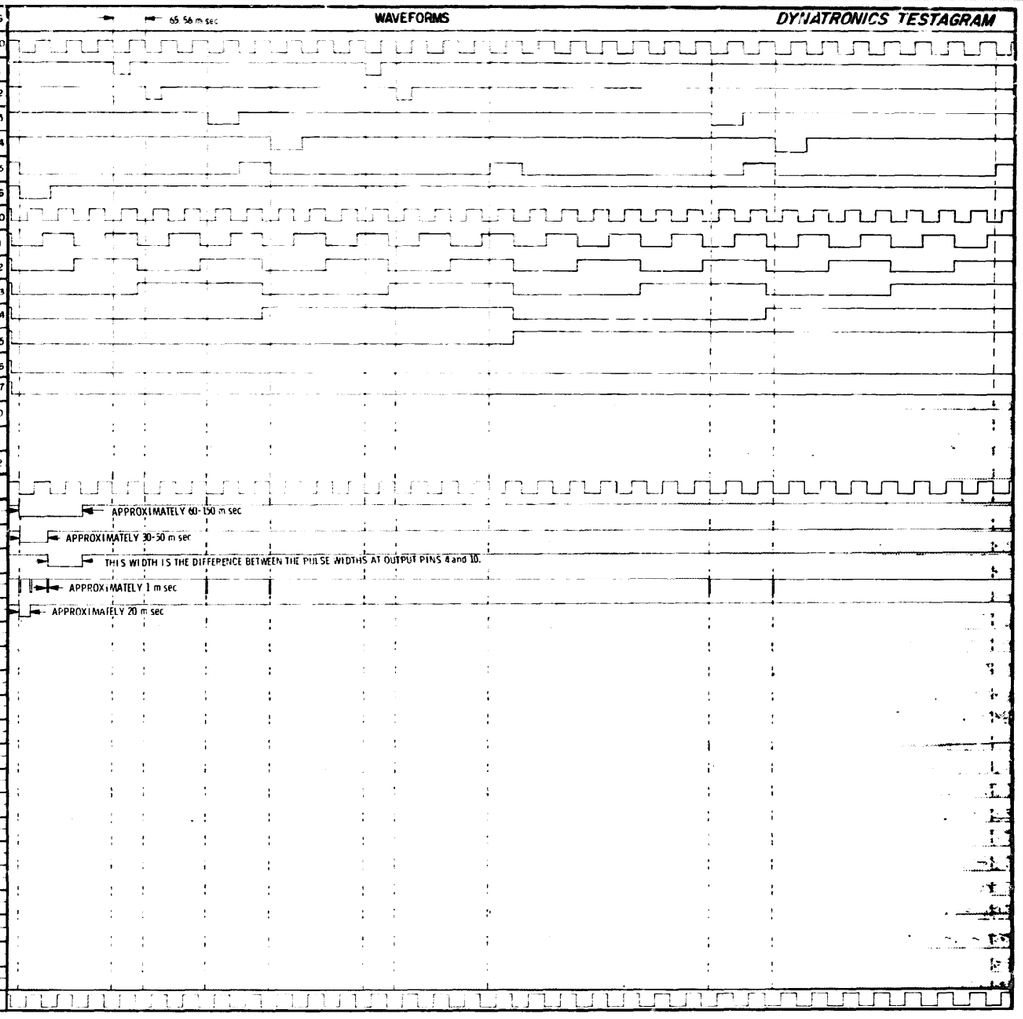
200075G1 DOC. NO. 23-2602-11

TEST PARAMETERS			
+Vcc	4.75	SIG V	GRD -V
±V	—	LOAD REF V	—
+V	12.0V	CLK	16.39 m sec
-V	12.0V	BIT CLK	÷OSC

ROW ASSIGNMENT	
10	—
1	—
2	+V
3	—
4	-V
5	GRD
6	—
7	-C6
8	-C3
9	-C4

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
1	
10.	
19	
20	
Q7 COLLECTOR	

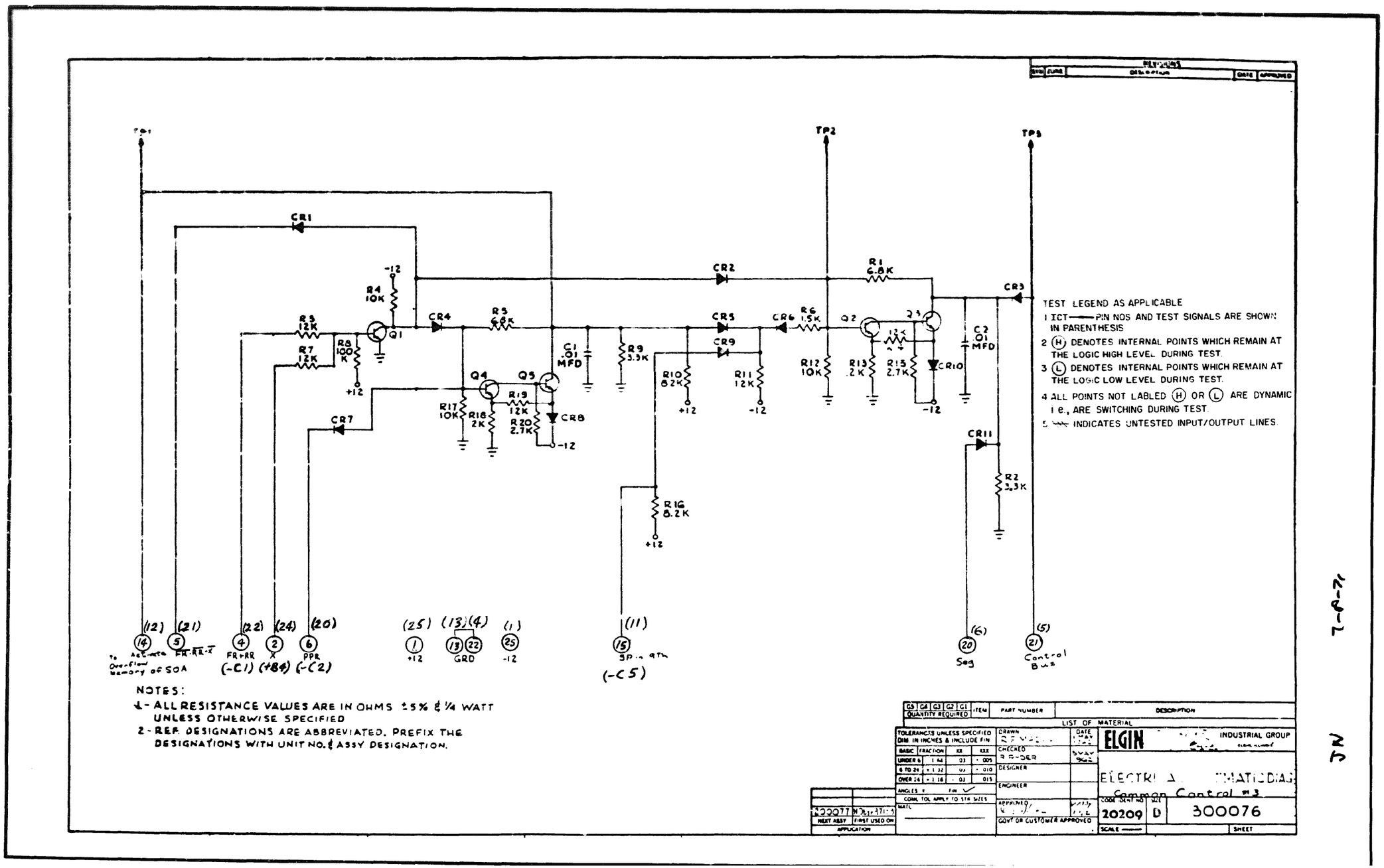
INPUT PINS		SIG
	63	+C0
	64	-C1
	65	-C2
23	66	-C3
24	67	-C4
	68	+C5
2	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+C0 REF



NOTE:

1. THIS CARD IS NOT GO/NO-GO TESTED. THE OUTPUTS CAN BE OBSERVED WITH AN OSCILLOSCOPE.

GOVT APPD. JW DATE 7-8-71



TEST LEGEND AS APPLICABLE

1 ICT——PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i e., ARE SWITCHING DURING TEST.
5 ~~ INDICATES UNTESTED INPUT/OUTPUT LINES.

NOTES:

1- ALL RESISTANCE VALUES ARE IN OHMS ±5% & ¼ WATT UNLESS OTHERWISE SPECIFIED
2- REF. DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION.

G5	G4	G3	G2	G1	ITEM	PART NUMBER	DESCRIPTION
QUANTITY REQUIRED							

LIST OF MATERIAL

TOLERANCES UNLESS SPECIFIED DIM IN INCHES & INCLUDE FIN			
BASIC	FRACTION	XX	XXX
UNDER 6	± .64	.03	± .005
6 TO 24	± 1.32	.03	± .010
OVER 24	± 1.16	.03	.015
ANGLES ±	FIN ✓		
COMM. TOL. APPLY TO STK SIZES			

DRAWN — DATE 1 MAY 72
CHECKED R. SNYDER — 5 MAY 72
DESIGNER
ENGINEER
APPROVED — 5/5/72
GOVT OR CUSTOMER APPROVED

ELGIN INDUSTRIAL GROUP

ELECTRICAL SCHEMATIC DIAG.
Common Control #3

CODE IDENT NO 20209 | SIZE D | 300076

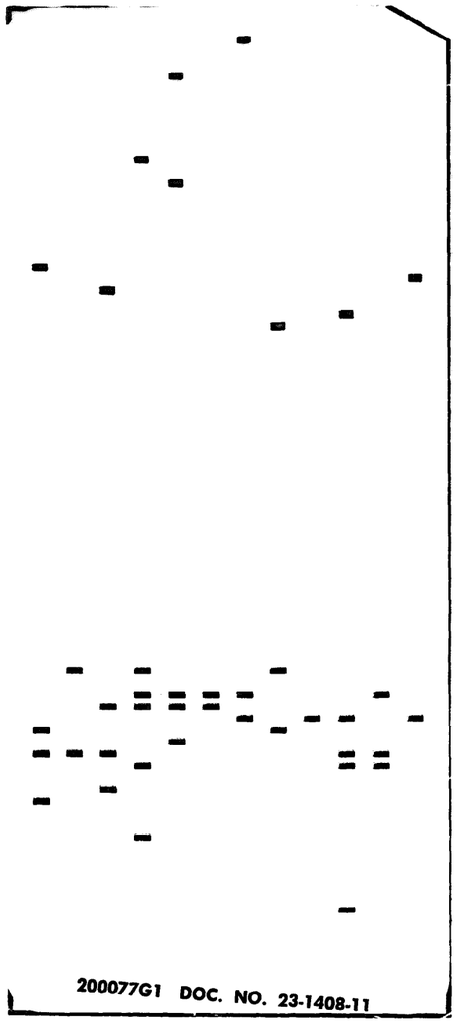
SCALE —— | SHEET

NEXT ASSY 200077 | FIRST USED ON Dwg 271-5

APPLICATION

MATL

7-9-72 JN



200077G1 DOC. NO. 23-1408-11

TEST PARAMETERS			
V_{cc}	4.75	S16 W LOAD INPUT	-12V
0V	-12V	CLR	16.39 m Sec
0V	+12V	BTCLR	+05C
-V	—		

PIN ASSIGNMENT	
10	+B4
1	—
2	+12V
3	-12V
4	—
5	GND
6	-C5
7	-C1
8	—
9	-C2

INPUT PINS		SIG
		+C0
22		-C1
39		-C2
		-C3
		-C4
38 *		-C5
		-C6
		+B0
		+B1
		+B2
		+B3
24		+B4
		+B5
		+B6
		+B7
		+S0
		+S1
		+S2

OUTPUT PINS (TEST POINTS)		SWITCH SETTING
21		
12	(1)	
6		
(5)	(3)	

+C0 REF

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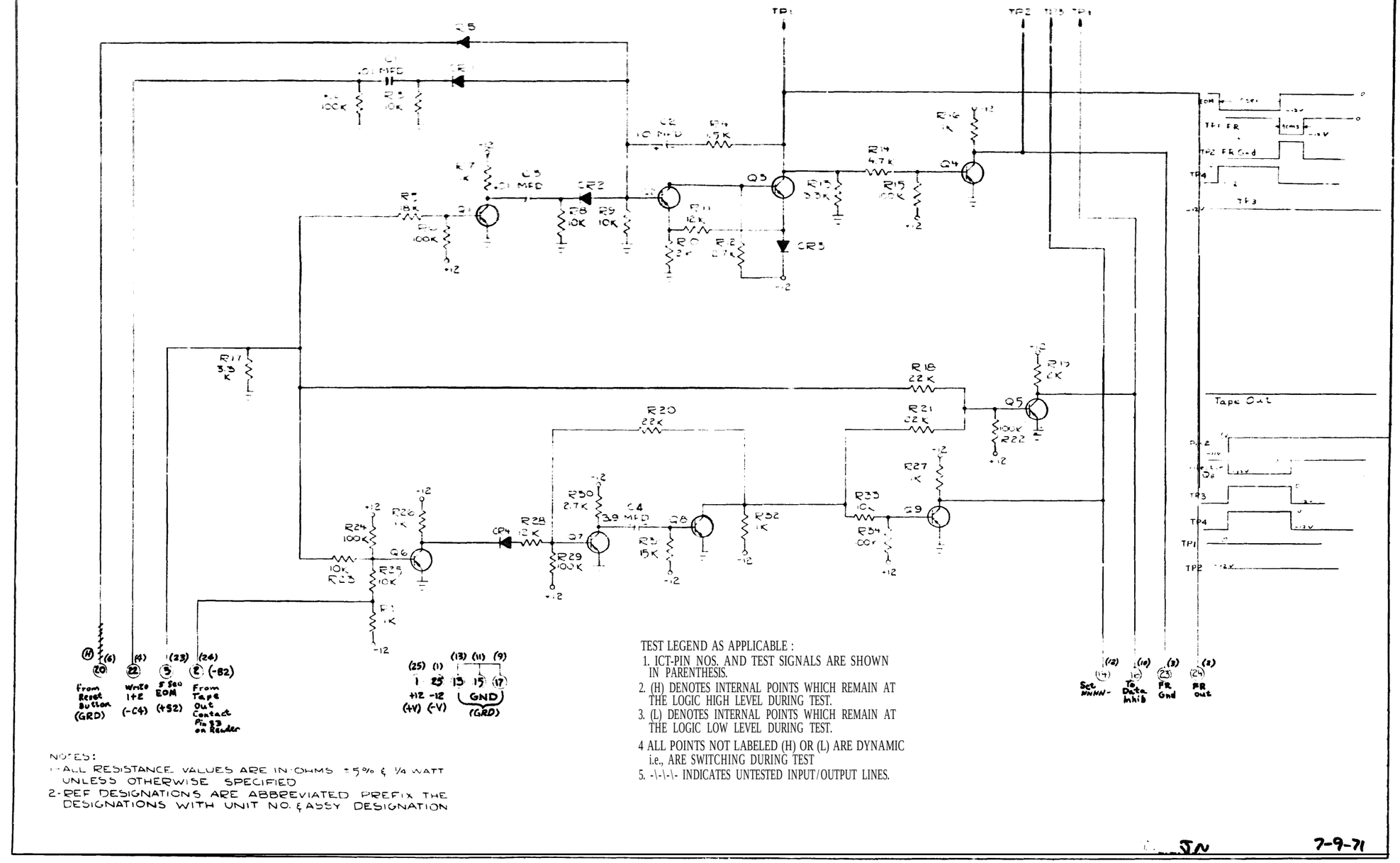
65.56 m Sec WAVEFORMS DYNATRONICS TESTAGRAM

NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. WAIT SEVERAL SECONDS FOR GO/NO-GO INDICATION.

GOVT APPD. JN DATE 7-8-71

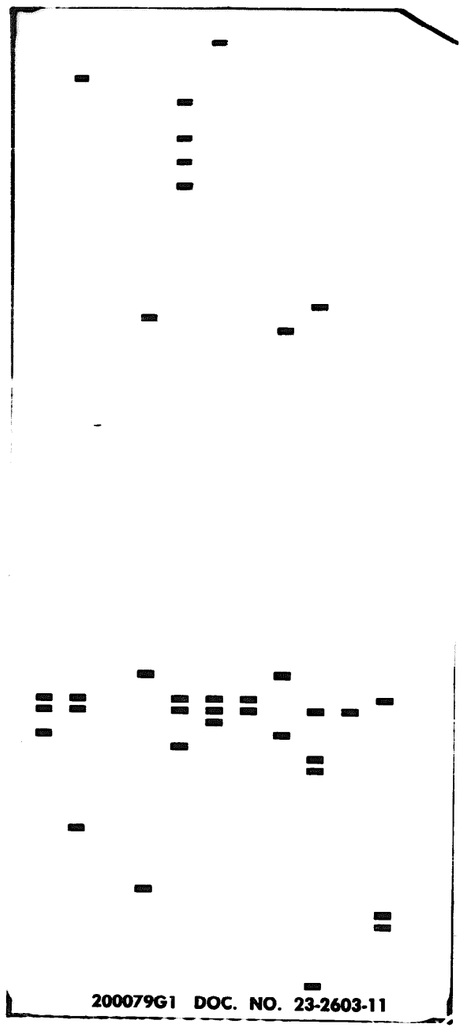


NOTES:
1-ALL RESISTANCE VALUES ARE IN OHMS ±5% & ¼ WATT UNLESS OTHERWISE SPECIFIED
2-REF DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION

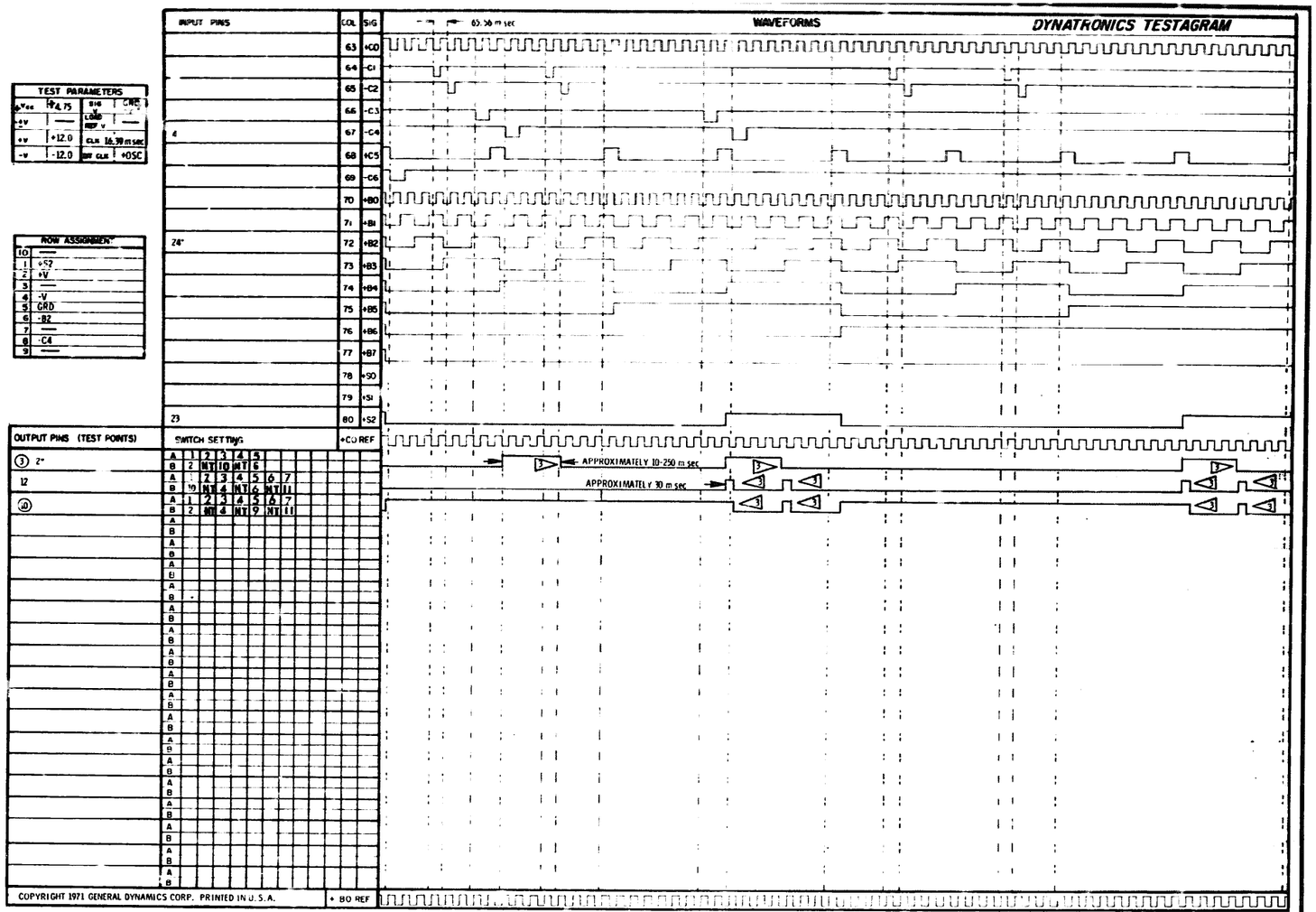
TEST LEGEND AS APPLICABLE :
1. ICT-PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST
5. -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES.

JN 7-9-71

P.C. Assembly 200079G1
P.C. Logic Navships 0967 216 3010 Doc. No. 23- 2603-11
Fig. 5-18



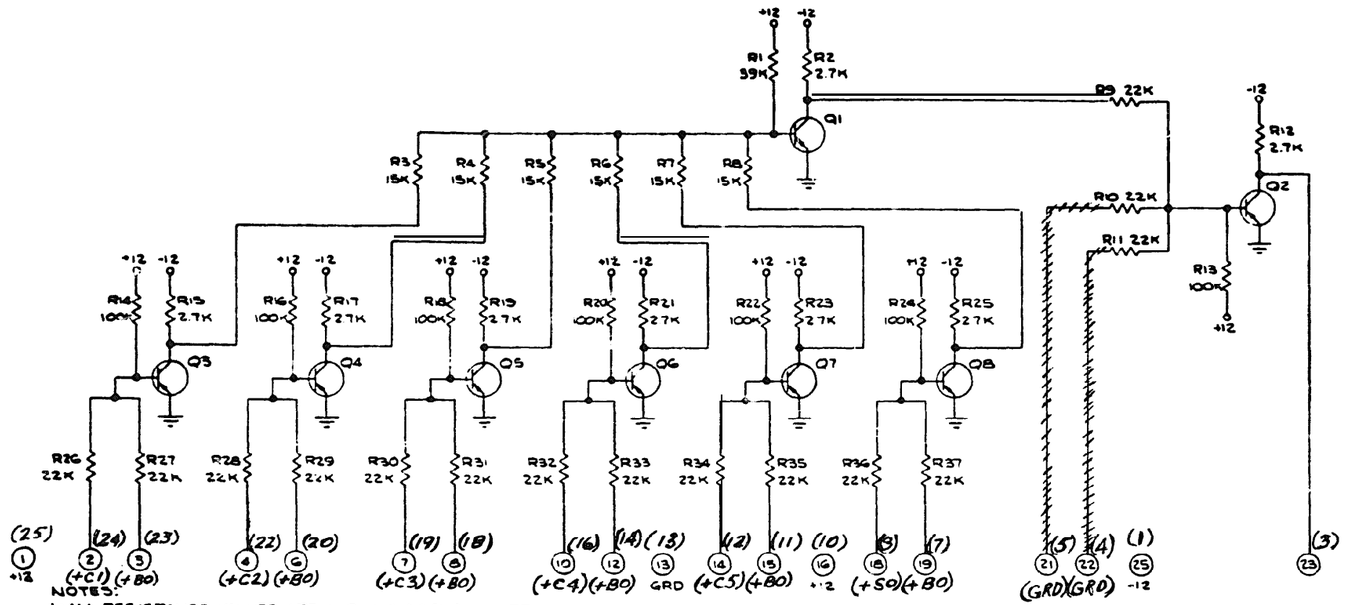
200079G1 DOC. NO. 23-2603-11



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. THESE EDGES ARE APPROXIMATE AND ARE NOT SYNCHRONOUS WITH THE TEST SIGNALS.
4. GO/NO-GO INDICATIONS REQUIRE SEVERAL SECONDS.
5. NT INDICATES NO TEST.

GOVT APPD. DN DATE 7-9-71



NOTES:
1-ALL RESISTANCE VALUES ARE IN OHMS ± 5% & ¼ WATT UNLESS OTHERWISE SPECIFIED
2-REF. DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION

TEST LEGEND AS APPLICABLE:

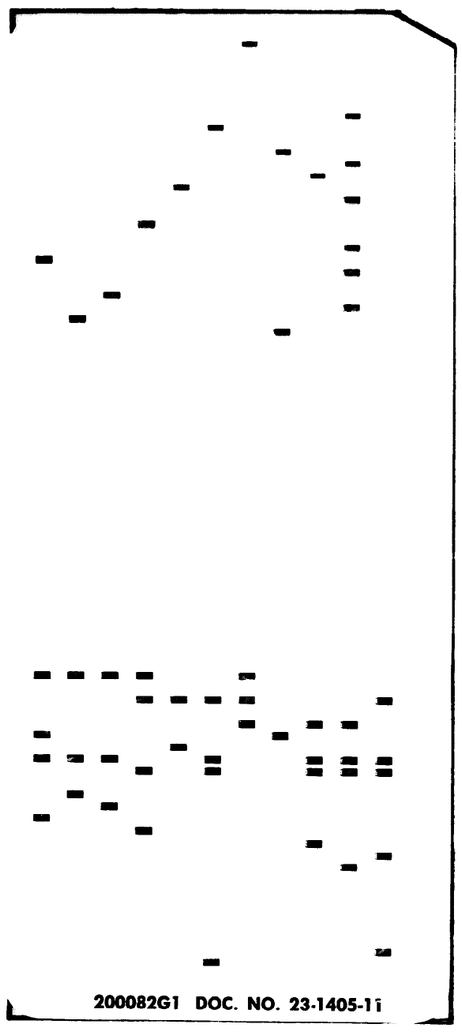
1. ICT- PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES.

GOVT APPD. JN 7-8-71

P.C. Assembly 200082 G1

P. C. Logic

Doc. No. 23- 1405 -11



200082G1 DOC. NO. 23-1405-11

TEST PARAMETERS			
V_{cc}	+4.75	SIG V	0 TO -12V
-v	-12	LOAD REF V	N/A
+v	+12	CLK	32μ sec
-v	—	INT CLK	+OSC

ROW ASSIGNMENT	
10	+B0
1	+C5
2	+12
3	-12
4	+S0
5	GND
6	-C4
7	+C2
8	+C1
9	+C3

INPUT PINS	COL	SIG
	63	+C0
24*	64	-C1
22*	65	-C2
19*	66	-C3
16*	67	-C4
12	68	+C5
	69	-C6
23, 20, 18, 14, 11, 1	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
8	78	+S0
	79	+S1
	80	+S2

WAVEFORMS — 128 μ S — DYNATRONICS TESTAGRAM

OUTPUT PINS (TEST POINTS)

3

SWITCH SETTING

	1	2	3	4	5	6	7	8	9	10	11	12
A	1	2	3	4	5	6	7	8	9	10	11	12
B	2	4	6	5	6	9	10	6	8	10	1	3

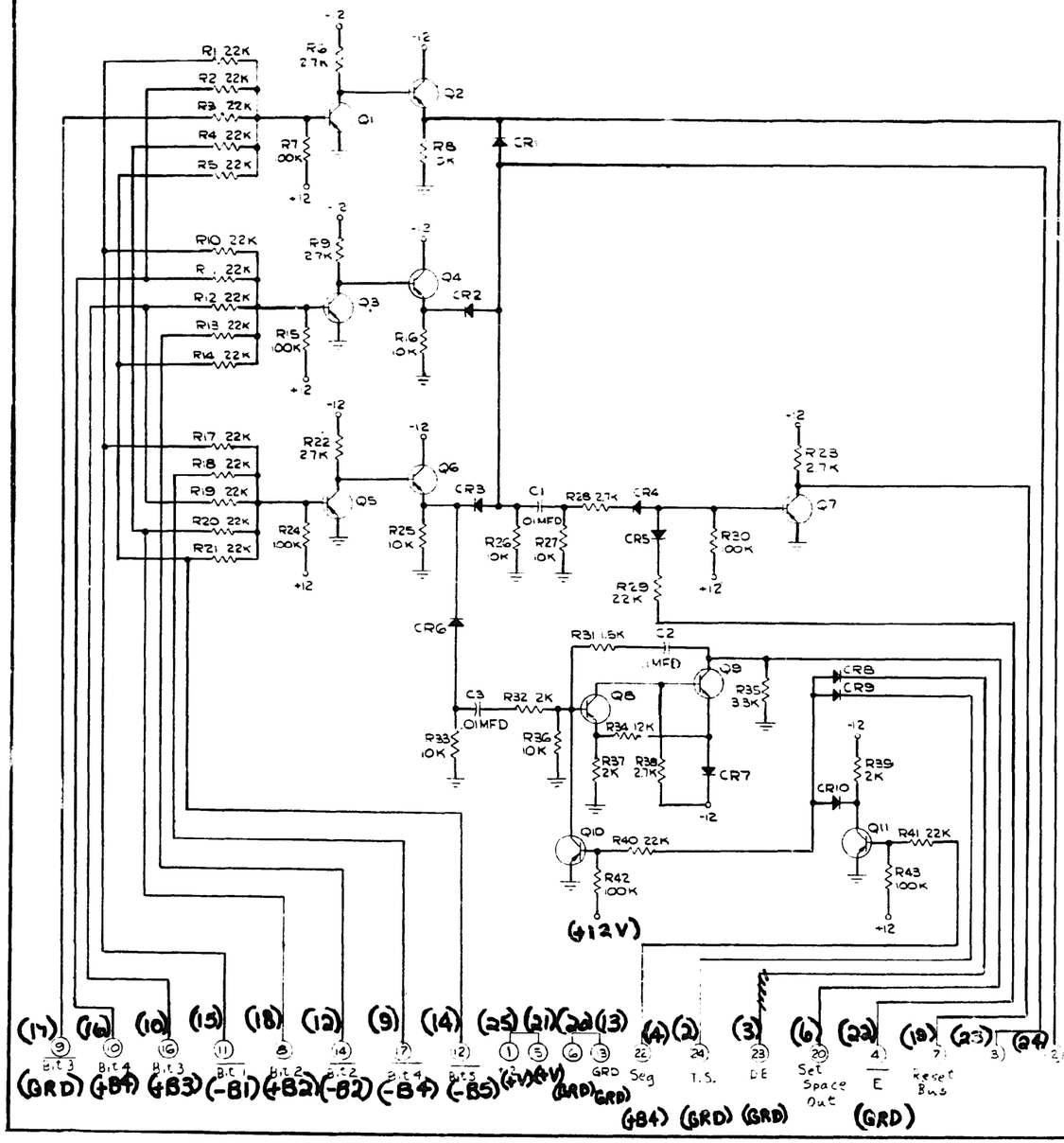
+C0 REF

+B0 REF

NOTES:

1. * DENOTES INVERTED INPUT.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

GOVT APPD. JN DATE 7-8-71

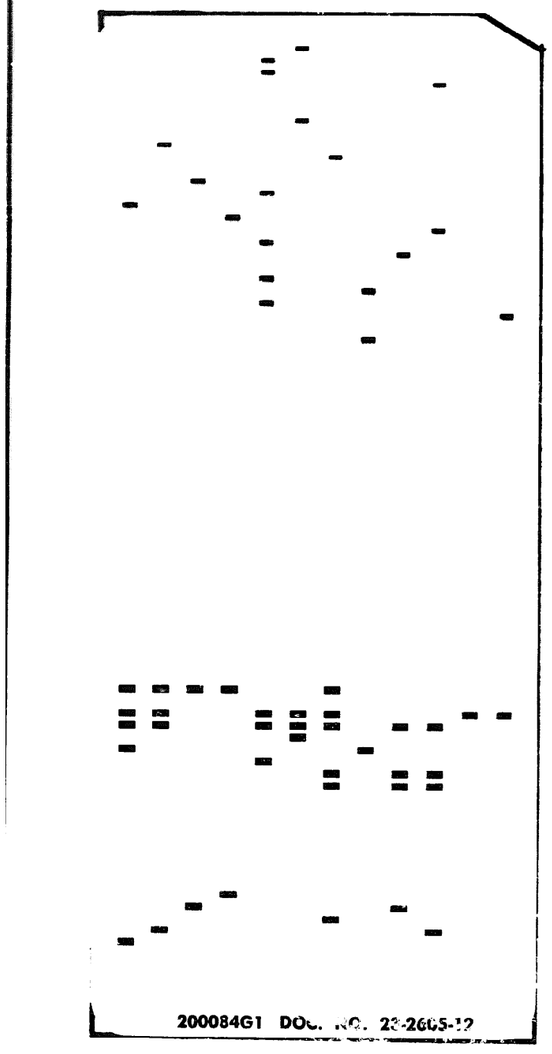


NOTES
1. ALL RESISTANCE VALUES ARE IN OHMS ± 2% ¼ WATT UNLESS OTHERWISE SPECIFIED
2. REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION

TEST LEGEND AS APPLICABLE:
1. ICT- PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ⫽⫽ INDICATES UNTESTED INPUT/OUTPUT LINES.

IN 7-8-71

P.C. Assembly 200084G1
P.C. Logic NAVSHIPS 0967 216 3010 Doc. No. 23-2605-12
Fig. 5-21

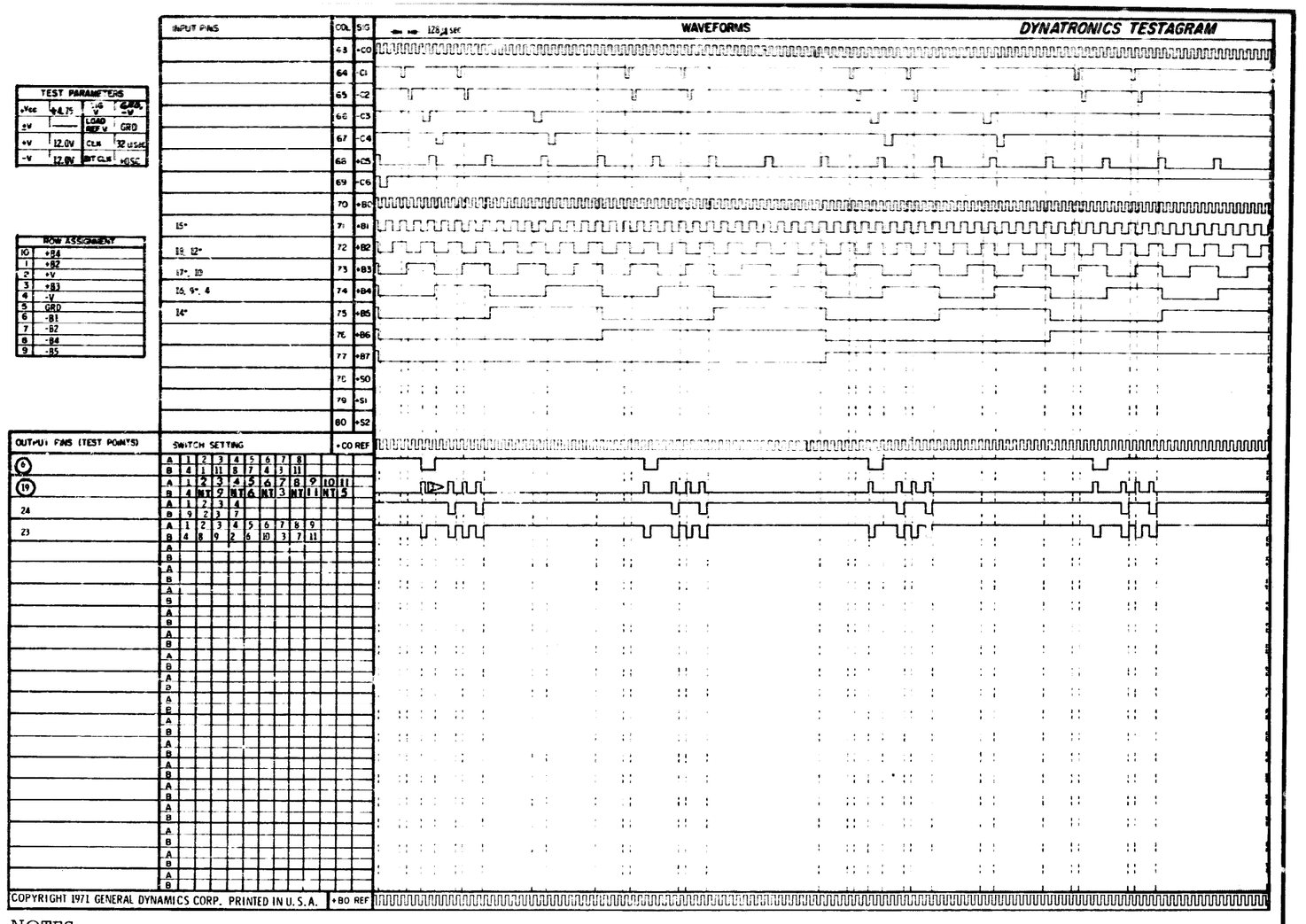


200084G1 DOC. NO. 23-2605-12

GOVT APPD. JN DATE 2-6-71

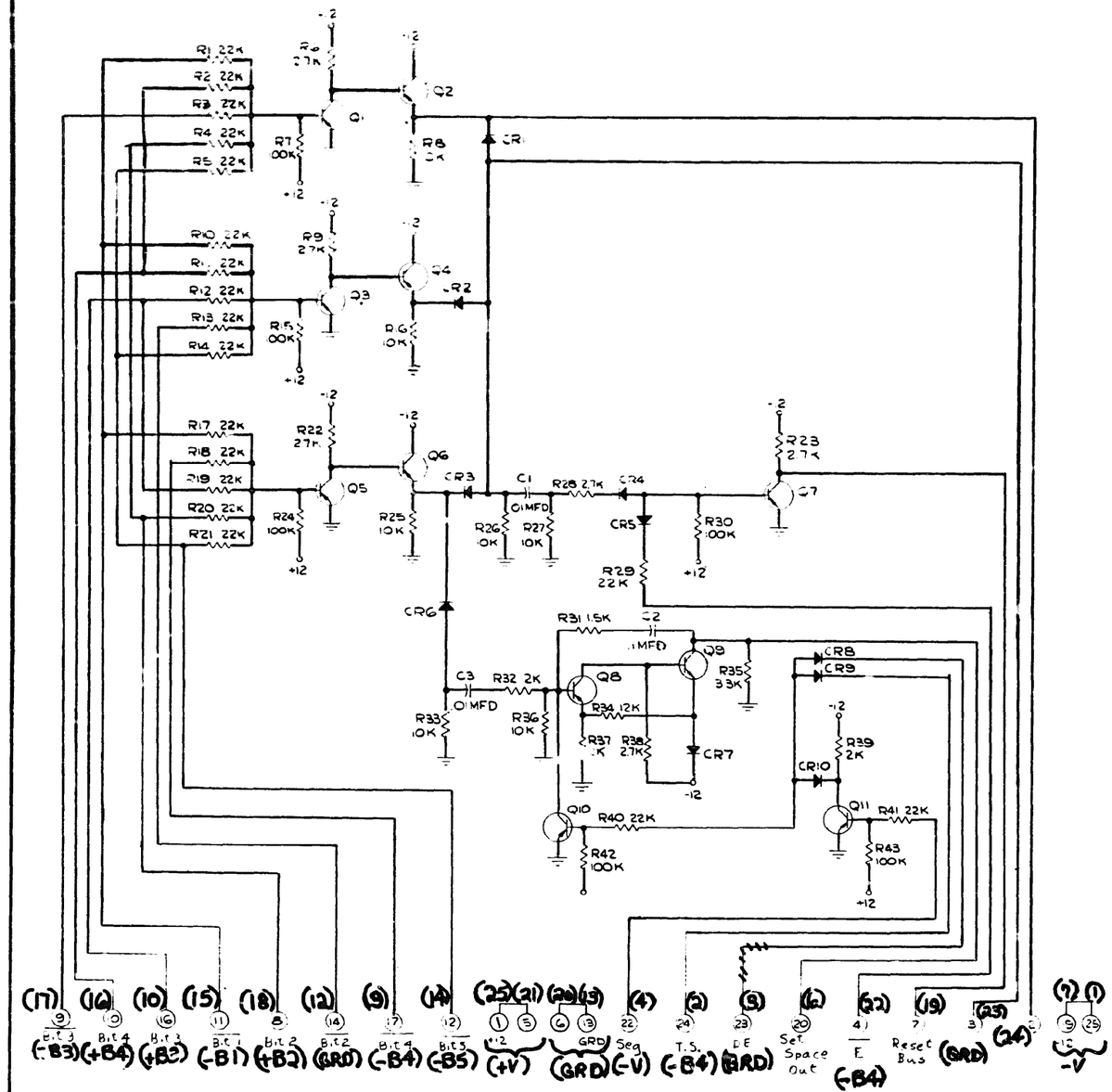
TEST PARAMETERS			
+Vcc	+4.75	LOAD REF V	GRD
±V	—	CLK	32 μsec
+V	12.0V	BIT CLK	+OSC
-V	12.0V		

ROW ASSIGNMENT	
10	+B4
1	+B2
2*	+V
3	+B3
4	-V
5	GRD
6	-B1
7	-B2
8	-B4
9	-B5



NOTES:

1. * DENOTES INVERTED SIGNAL.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
3. THE TRAILING EDGES ARE NOT SYNCHRONOUS WITH THE TEST WAVEFORMS.
4. NT INDICATES NO TEST.



NOTES
1- ALL RESISTANCE VALUES ARE IN OHMS ± 5% ¼ WATT UNLESS OTHERWISE SPECIFIED
2- REF DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION

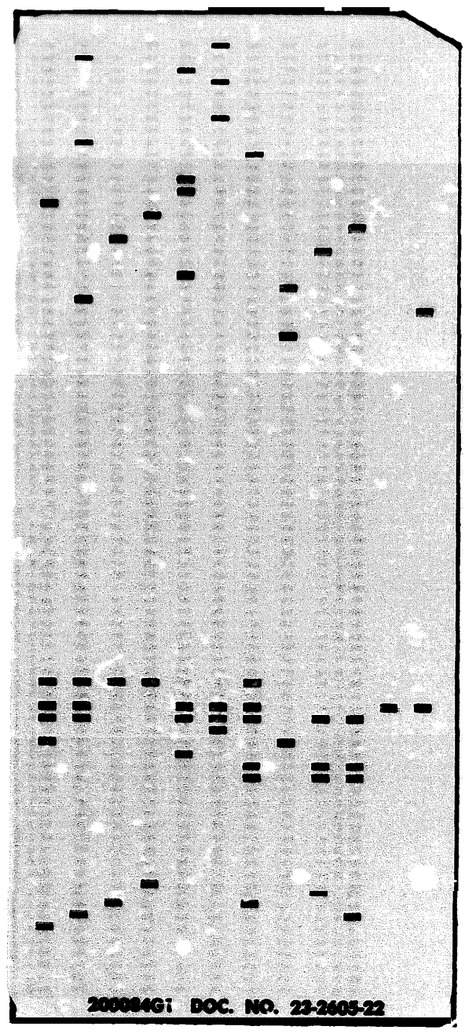
TEST LEGEND AS APPLICABLE:
1. ICT—— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ⟋⟋ INDICATES UNTESTED INPUT/OUTPUT LINES.

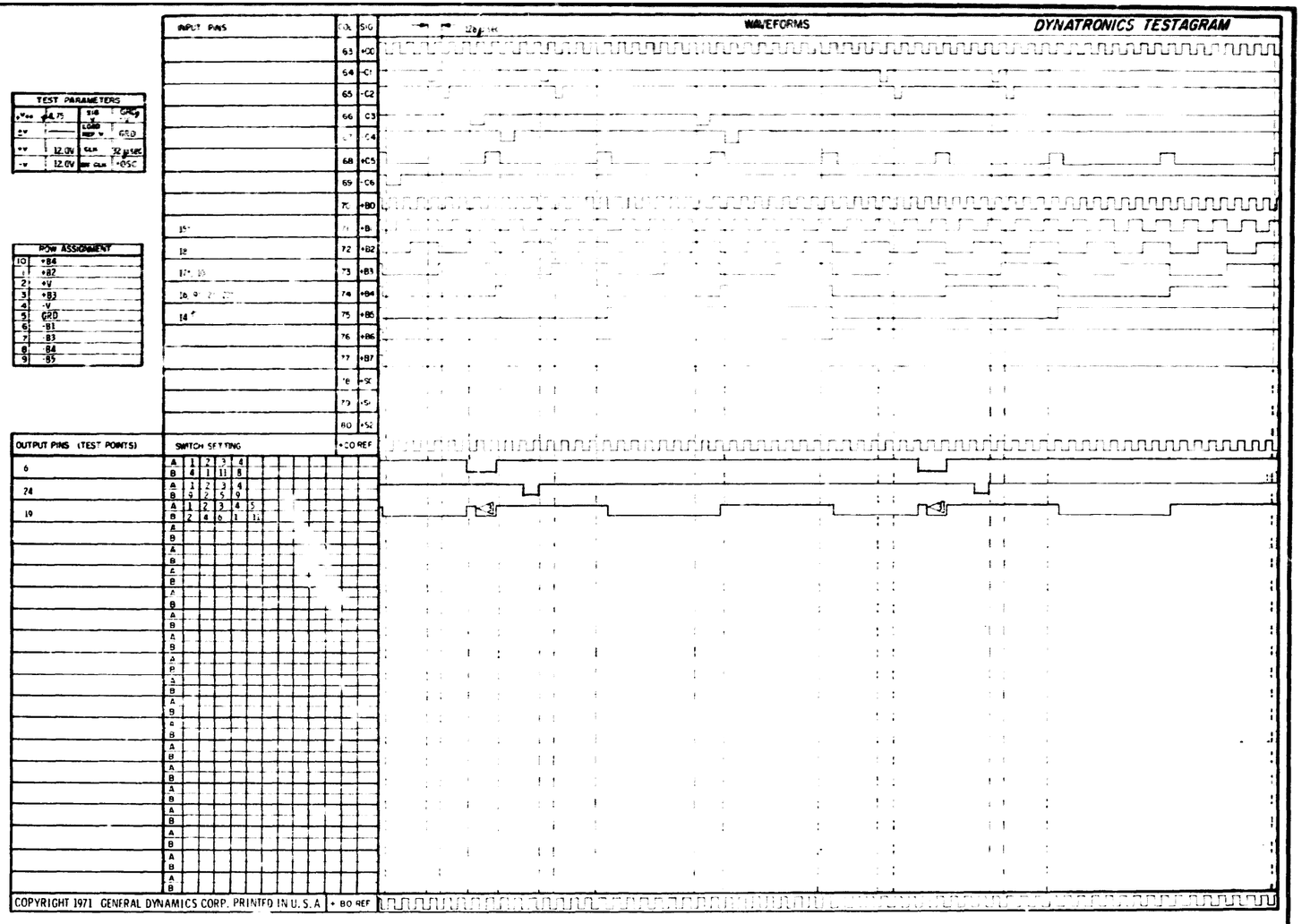
JN 2-8-71

P.C. Assembly 200084G1
P.C. Logic NAVSHIPS 0967 216 3010

Doc. No. 23-2605-22

Fig. 5-21





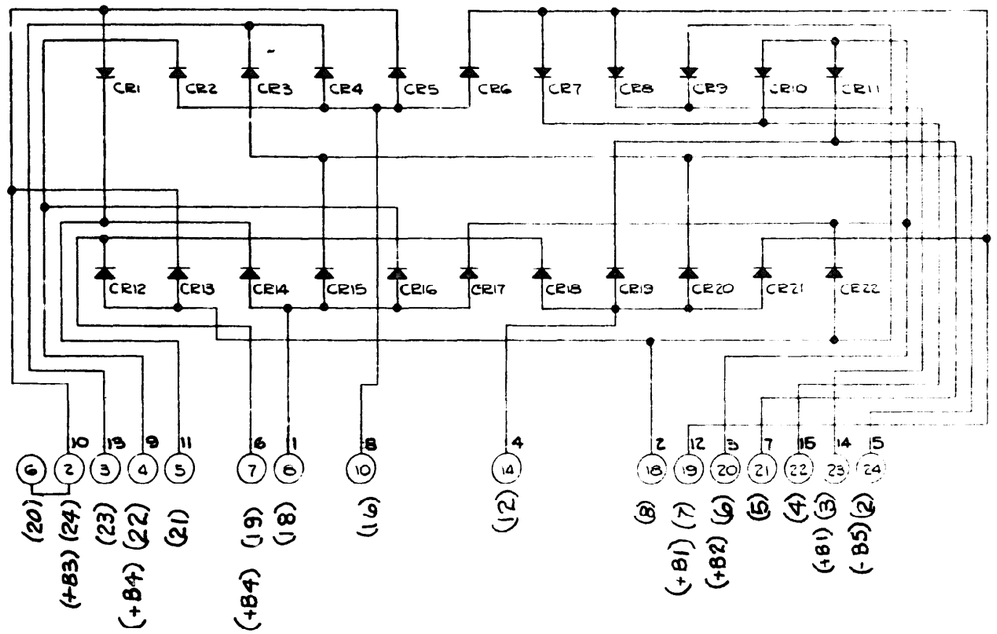
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
3. THIS EDGE IS NOT SYNCHRONOUS WITH THE TEST WAVEFORMS.

GOVT APPD. JN DATE 2-8-71

TEST LEGEND AS APPLICABLE

1. ICT----PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN Al THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST
5 -\-\-\- INDICATES UNTESTED INPUT/OUTPUT LINES



EXAMPLE

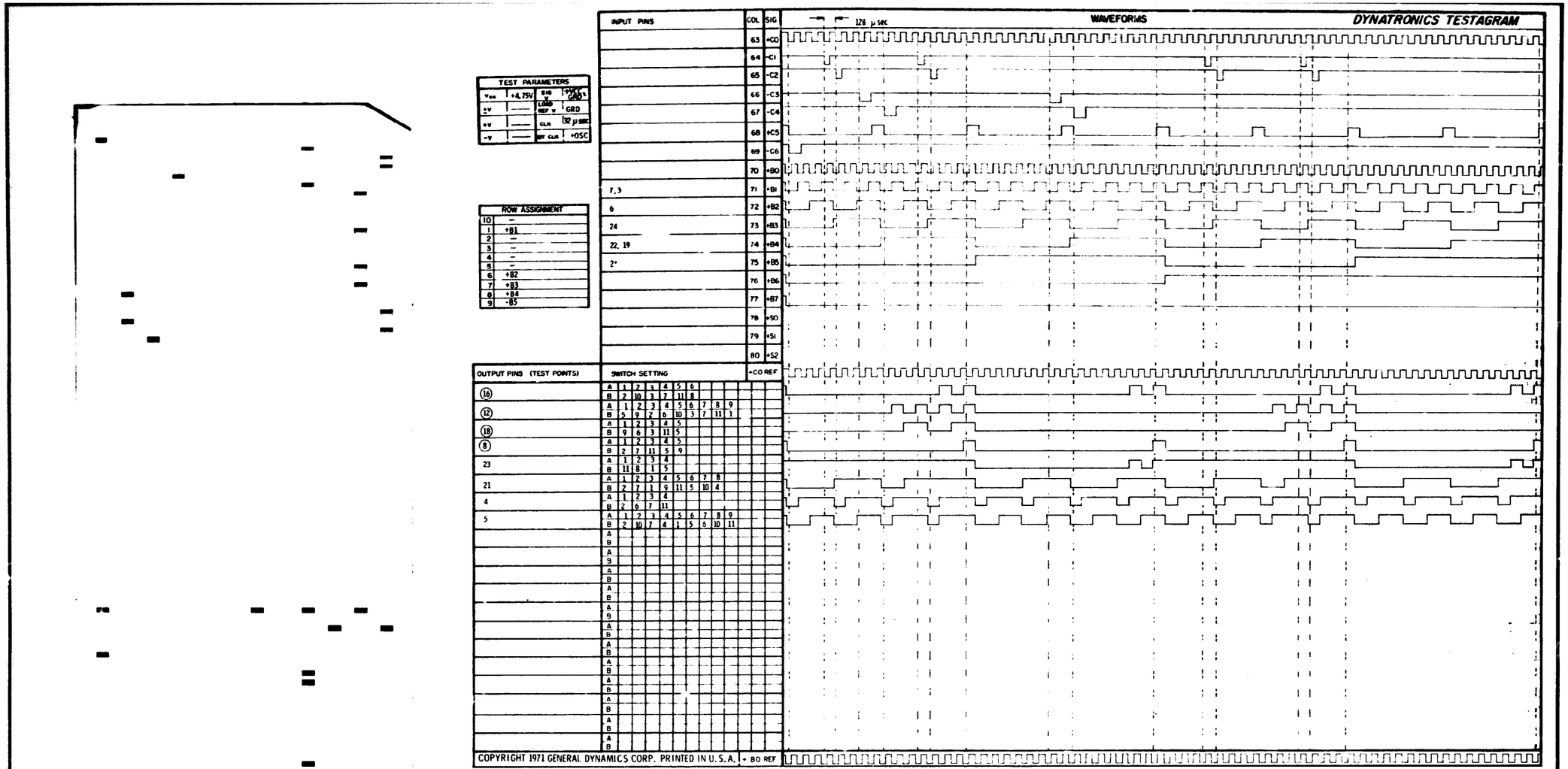
INPUT -12V ON PIN 5
BINARY 11

OUTPUT -12V ON PIN 8
BINARY 1
-12V ON PIN 18
BINARY 2
0V ON PIN 14
NO BINARY 4
-12V ON PIN 10
~~BINARY 8~~
BINARY 11

JW 7-8-71

P.C. Assembly 200086G1

P.C. Logic NAVSHIPS 0967 216 3010 Doc. No. 23- 2609-11
Fig. 5-25

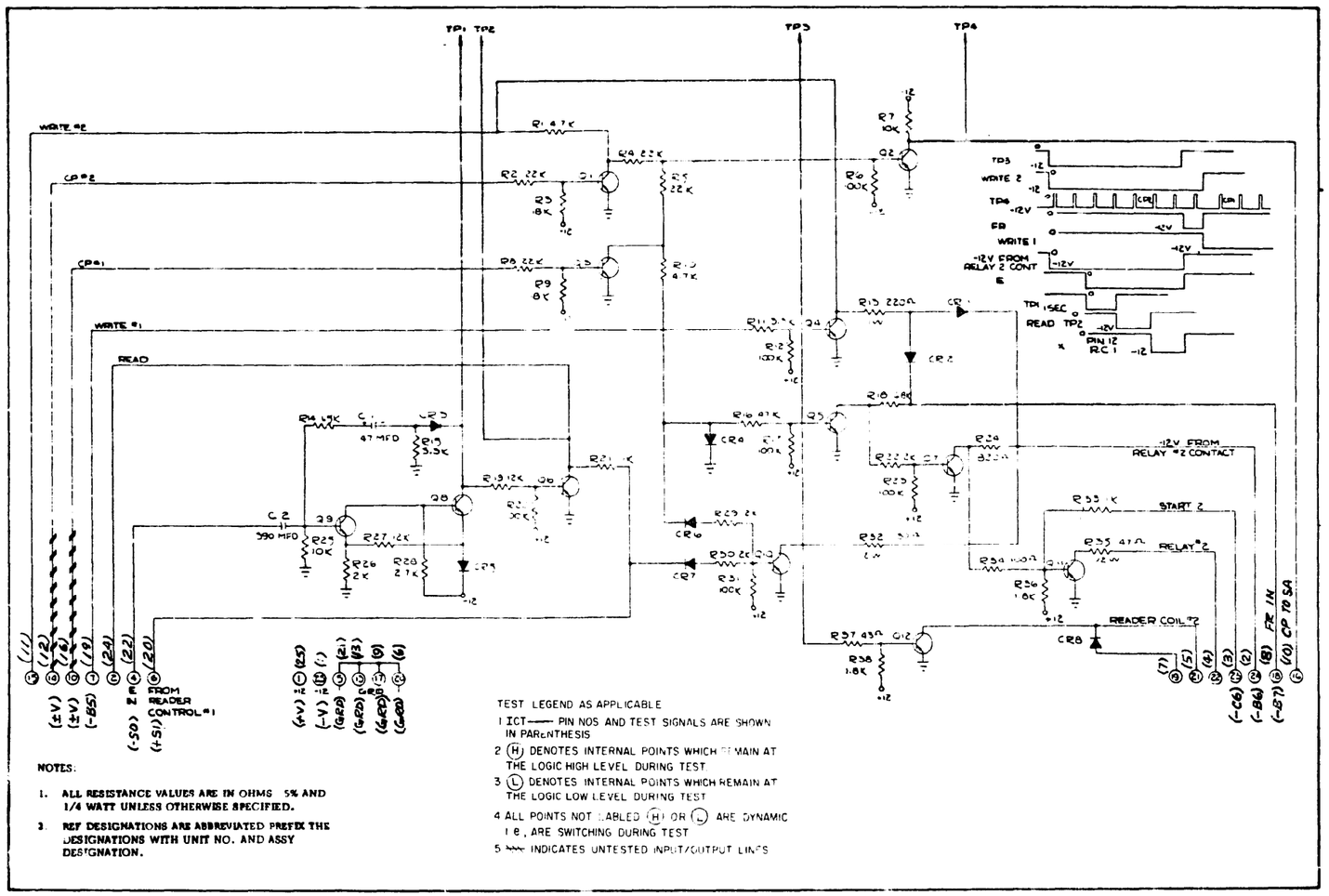


NOTES:

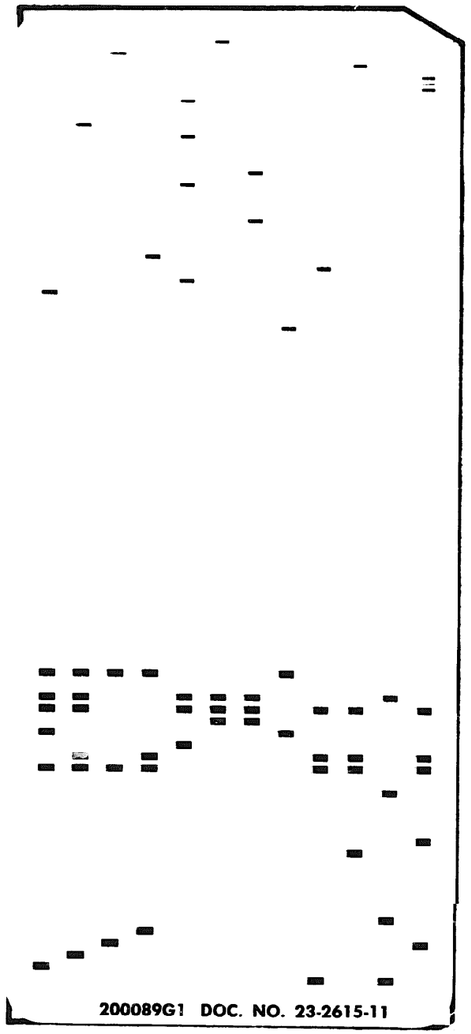
1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

P.C. 200086G1 DOC. NO. 23-2609-11

GOVT APPD. JW DATE 2-9-71


TP1 TP2
TP3
TP4
WRITE #2
CP#2
CP#1
WRITE #1
READ
R1 4.7K
R2 22K
R3 8K
R4 22K
R5 22K
R6 8K
R7 10K
R8 4.7K
R9 8K
R10 220Ω
R11 3.3K
R12 100K
R13 3.3K
R14 4.7K
R15 3.3K
R16 47K
R17 100K
R18 47Ω
R19 12K
R20 2.7K
R21 1K
R22 2K
R23 10K
R24 33Ω
R25 100K
R26 2K
R27 12K
R28 2K
R29 100K
R30 33Ω
R31 100K
R32 5.1Ω
R33 1K
R34 100Ω
R35 47Ω
R36 1.8K
R37 47Ω
R38 1.8K
C1 47 MFD
C2 390 MFD
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
+12
-12
TP3
WRITE 2
TP6
+12V
FR
WRITE 1
-12V FROM RELAY 2 CONT E
TP1 1SEC
READ TP2
PIN 12 RC 1
-12V FROM RELAY #2 CONTACT
START 2
RELAY #2
READER COIL #2
FROM READER CONTROL #1
FR IN
CP TO SA
TEST LEGEND AS APPLICABLE
1 ICT—— PIN NOS AND TEST SIGNALS ARE SHOWN IN PARENTHESIS
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC I.E., ARE SWITCHING DURING TEST
5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES
NOTES:
1. ALL RESISTANCE VALUES ARE IN OHMS 5% AND 1/4 WATT UNLESS OTHERWISE SPECIFIED.
3. REF DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH UNIT NO. AND ASSY DESIGNATION.

APPD. _____ DATE _____



200089G1 DOC. NO. 23-2615-11

TEST PARAMETERS			
+Vcc	4.75	SIG V	GRD
±V	+18V	LOAD REF V	-V
+V	12.0V	CLK 16.39 m sec	
-V	12.0V	BIT CLK	+OSC

ROW ASSIGNMENT	
10	-C6
1	+S1
2	+V
3	±V
4	-V
5	GRD
6	-B5
7	-B6
8	+B7
9	-S0

INPUT PINS	COL	SIG
	63	+C0
	64	C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
3	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
19*	75	+B5
2*	76	+B6
8*	77	+B7
22*	78	+S0
20	79	+S1
	80	+S2
SWITCH SETTING		+C0 REF

OUTPUT PINS (TEST POINTS)

24

5, 7

④

⑩

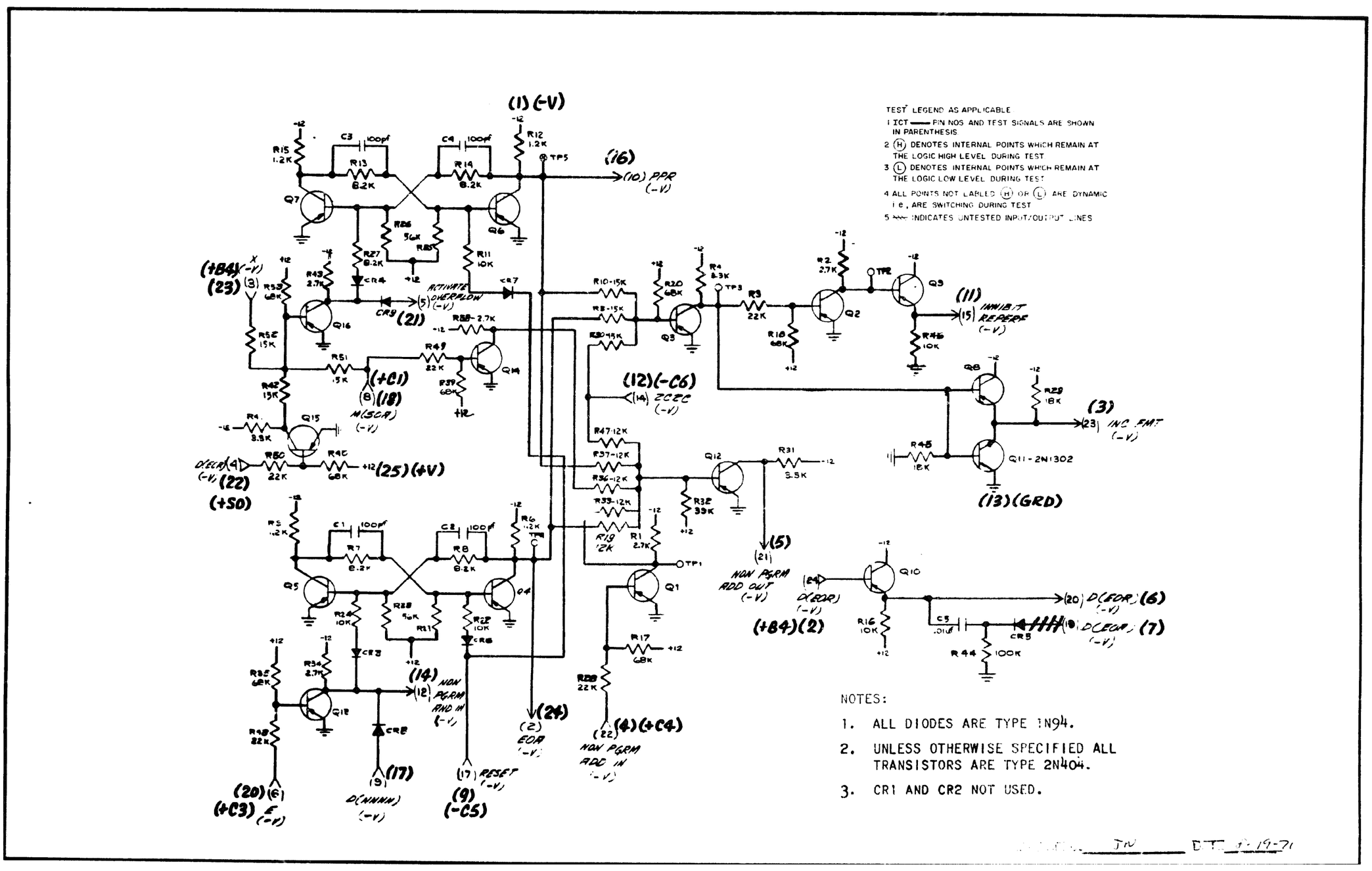
WAVEFORMS — 65.50 m sec — DYNATRONICS TESTAGRAM

+B0 REF

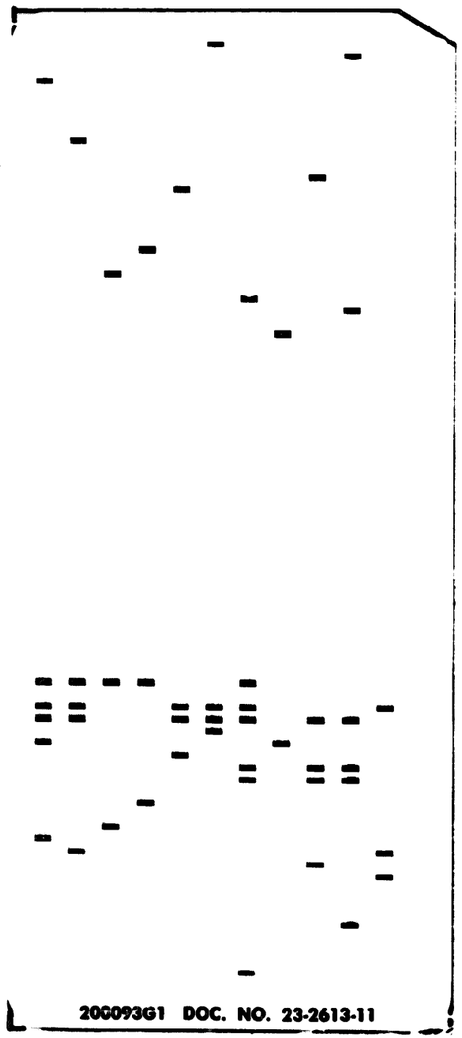
NOTES :

1. * DENOTES INVERTED SIGNAL.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
3. THIS EDGE IS NOT SYNCHRONOUS WITH THE TEST WAVEFORMS. THE LOCATION OF THIS EDGE VARIES FROM CARD TO CARD.
4. NT INDICATES NO TEST.

GOVT APPD._____ DATE_____



P.C. Assembly 200093G1 Doc. No. 23-2613-11
P.C. Logic NAVSHIPS 0967 216 3010
Fig. 5-66



200093G1 DOC. NO. 23-2613-11

TEST PARAMETERS			
V_{cc}	+4.75V	SIG	GRD, -V
±V	—	LOAD	V
+V	12.0V	CLK	2 µSEC
-V	12.0V	REF CLK	+OSC

ROW ASSIGNMENT	
10	+B4
1	-C6
2	+Y
3	+S0
4	-V
5	GRD
6	+C1
7	+C3
8	-C5
9	+C4

OUTPUT PINS (TEST POINTS)
⑤
③ 11*
24
16
6
21
14, 17

INPUT PINS	COL	SIG
	63	+C0
18*	64	-C1
	65	-C2
20*	66	-C3
4*	67	-C4
9*	68	+C5
12	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
23	74	+B4
	75	+B5
	76	+B6
	77	+B7
22	78	+S0
	79	+S1
	80	+S2

SWITCH SETTING

A	1	2	3	4	5	6	7	8	9	10	11	
B	3	7	4	6	5	9	2	6	3	8	3	
A	1	2	3	4	5	6	7	8				
B	3	7	5	9	4	8	3	7				
A	1	2	3	4								
B	5	9	3	7								
A	1	2	3	4								
B	4	8	11	4								
A	1	2	3	4								
B	2	1	11	10								
A	1	2	3	4								
B	4	5	11	1								
A	1	2	3	4								
B	5	9	3	7								
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												
A												
B												

WAVEFORMS — DYNATRONICS TESTAGRAM

+CO REF

+80 REF

NOTES:

1. * DENOTES INVERTED SIGNAL
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

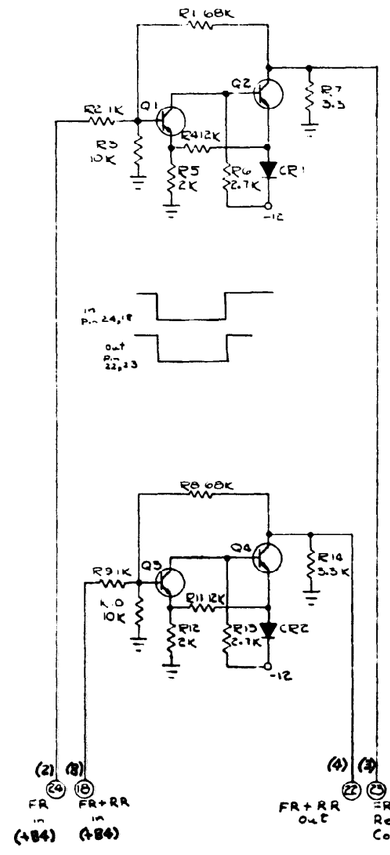
GOVT APPD. JW DATE 8-19-71

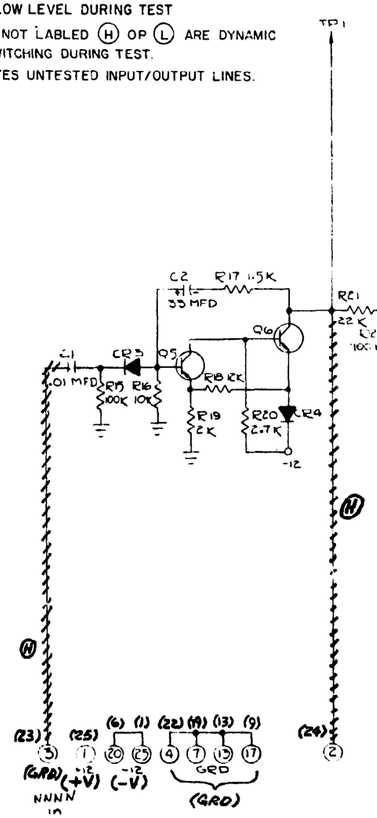
Doc. No. 23-2613-11

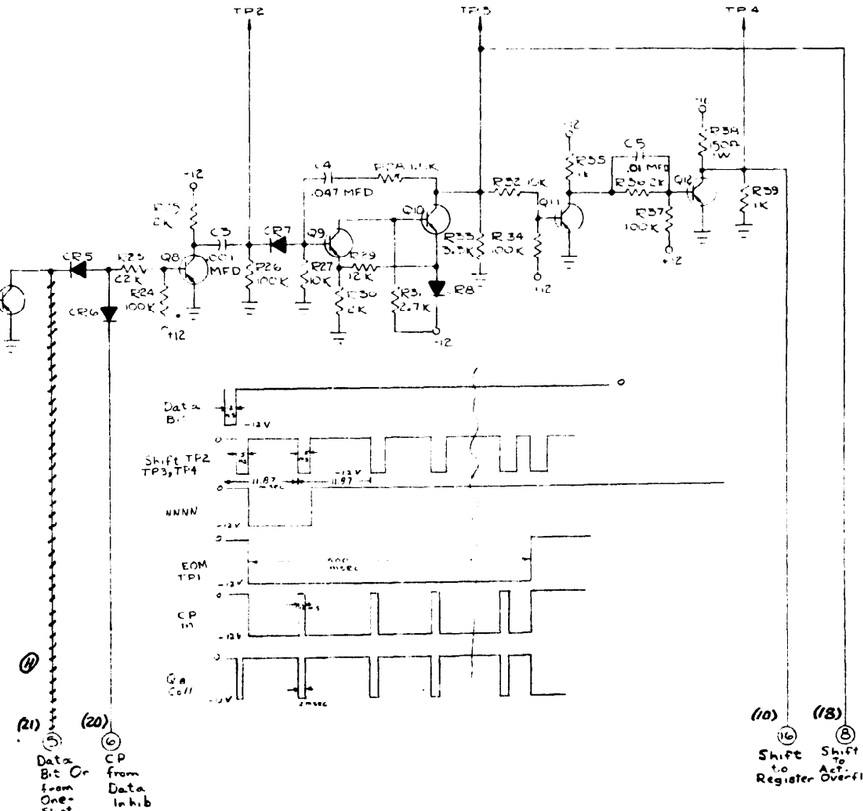
P.C. Assembly 200095G1
P.C. Logic NAVSHIPS 0967 216 3010
Fig. 5-66

TEST LEGEND AS APPLICABLE:

1. ICT—— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ⋙ INDICATES UNTESTED INPUT/OUTPUT LINES.



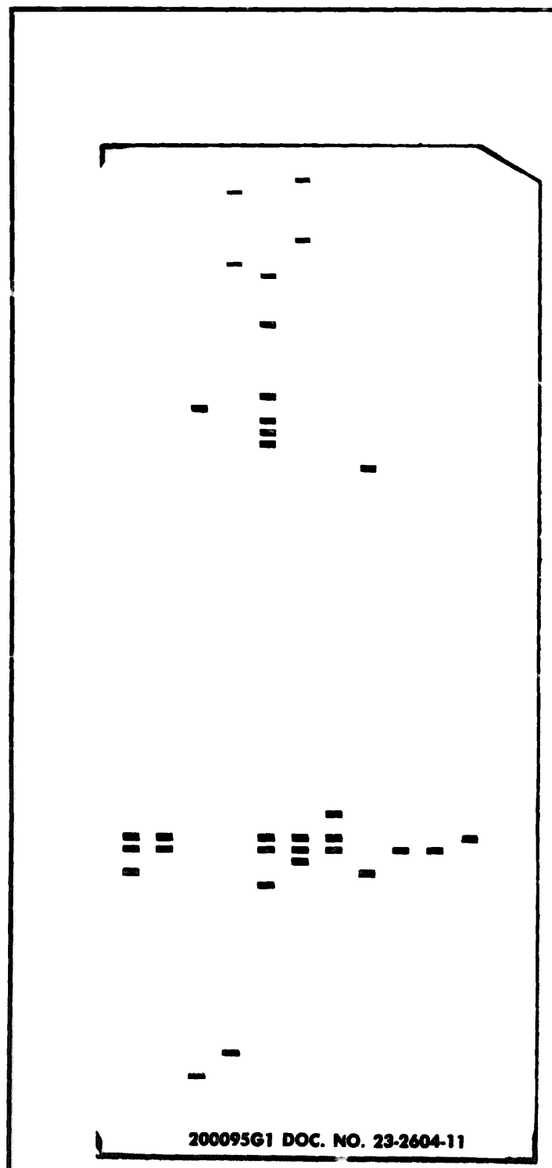




NOTES:
1-ALL RESISTANCE VALUES ARE IN OHMS ±5% ¢ ¼ WATT UNLESS OTHERWISE SPECIFIED
2-REF DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH UNIT NO. & ASSY DESIGNATION

7-9-71

P.C. Assembly 200095G1 Doc. No. 23-2604-11
P.C. Logic NAVSHIPS 0967 216 3010



200095G1 DOC. NO. 23-2604-11

TEST PARAMETERS			
V_{OH}	4.75	T1 / LOAD TO V	GRD. -V
±V	—		—
+V	12.0V	CLK	32 μ sec
-V	12.0V	BIT CLK	+OSC

ROW ASSIGNMENT	
10	—
1	—
2	+V
3	—
4	-V
5	GRD
6	+B4
7	+B6
8	—
9	—

OUTPUT PINS (TEST POINTS)
4, 3
18, 10

SWITCH SETTING				
A	1	2	3	4
B	2	1	11	10
A	1	2	3	
B	9	NT	1	

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
2, 8	74	+B4
	75	+B5
20	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+CO REF

WAVEFORMS — DYNATRONICS TESTAGRAM

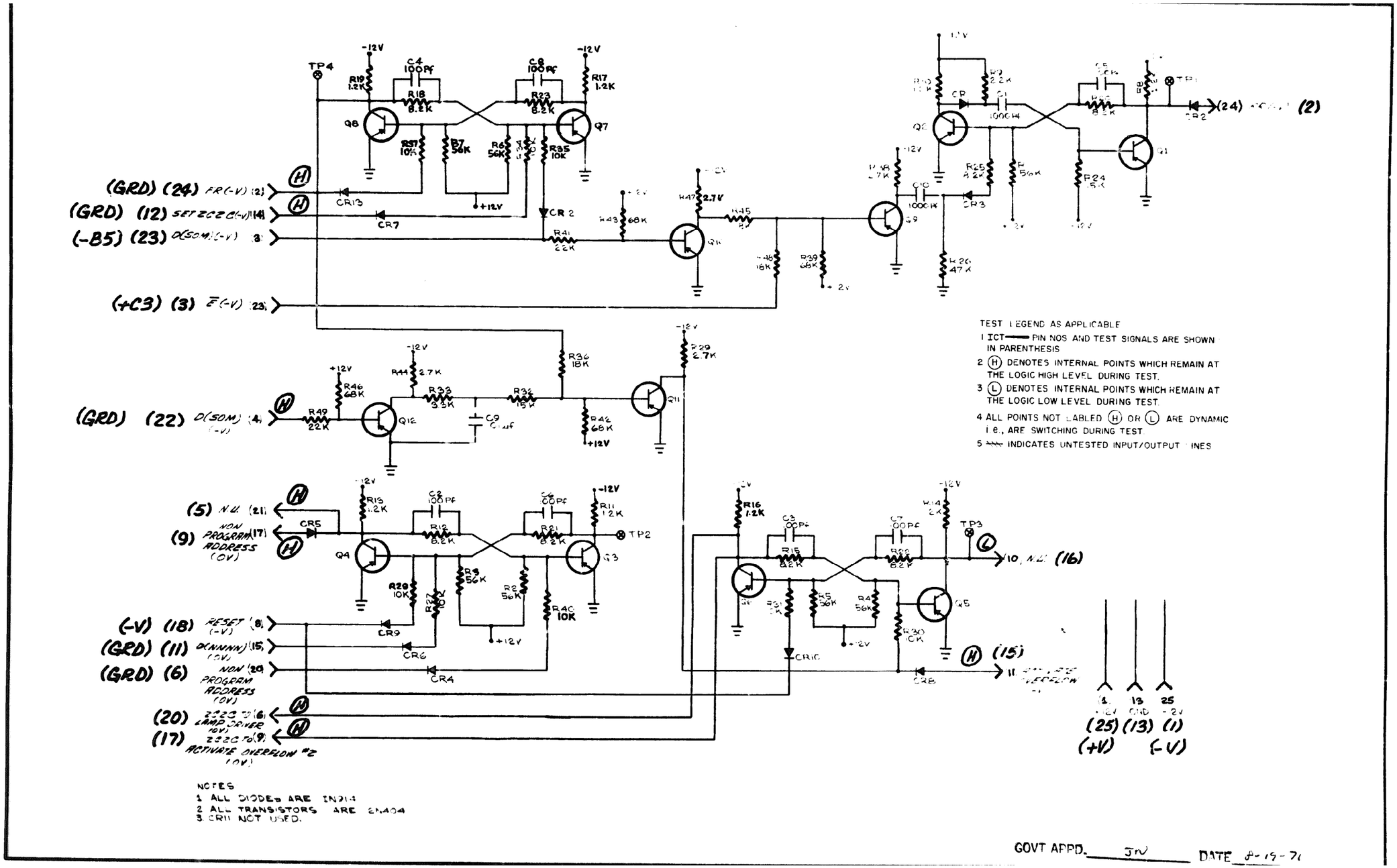
← → 128 μ sec

← APPROXIMATELY 0.5 TO 1.0 m sec

NOTES:

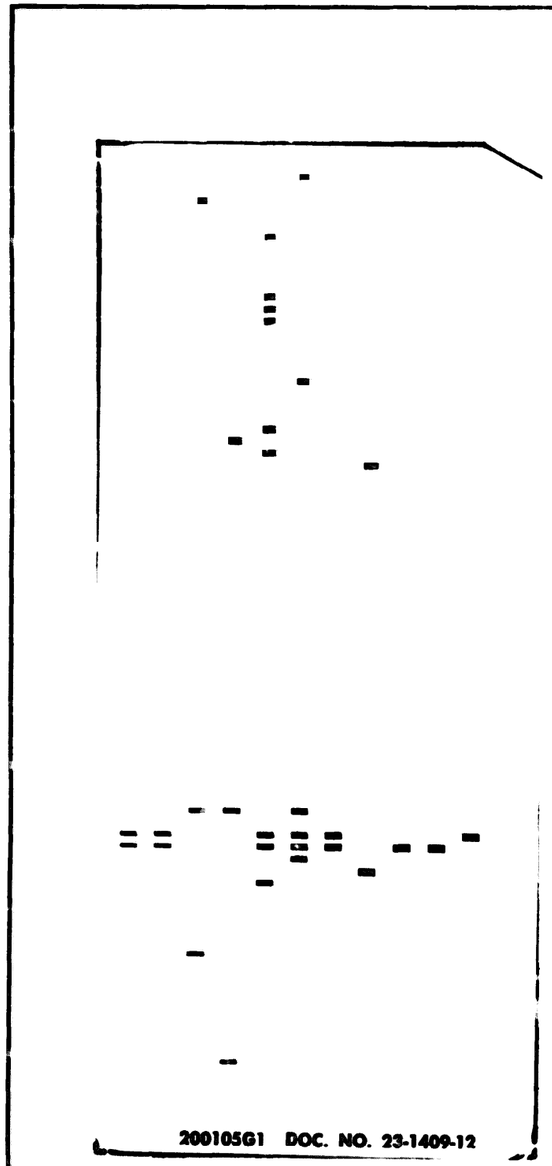
1. * DENOTES INVERTED SIGNAL.
2. THE WIDTH OF THIS PULSE VARIES BETWEEN CARDS. THE TRAILING EDGE IS NOT SYNCHRONOUS WITH THE TEST SIGNALS.
3. NT INDICATES NO TEST.

GOVT APPD. JN DATE 7-9-71



P.C. Assembly 200105G1
P.C. Logic NAVSHIPS 0967 216 3010
Fig. 5-62

Doc. No. 23-1409-12



200105G1 DOC. NO. 23-1409-12

TEST PARAMETERS

V_{CC}	+4.75V	8/16	GRD, -V
±V		LOAD +12.0 V	
+V	12.0V	CLK	2 µ sec
-V	12.0V	BIT CLK	

ROW ASSIGNMENT

10	—
1	—
2	+V
3	—
4	-V
5	GRD
6	-B3
7	+C3
8	—
9	—

INPUT PINS

3*

23*

OUTPUT PINS (TEST POINTS)

2

SWITCH SETTING

A/B	1	2	3	4	5
			NT	NT	+V

COL	SIG
63	+C0
64	-C1
65	-C2
66	-C3
67	-C4
68	+C5
69	-C6
70	+B0
71	+B1
72	+B2
73	+B3
74	+B4
75	+B5
76	+B6
77	+B7
78	+S0
79	+S1
80	+S2
	+C0 REF
	+20 REF

WAVEFORMS — ← 8 µ sec →

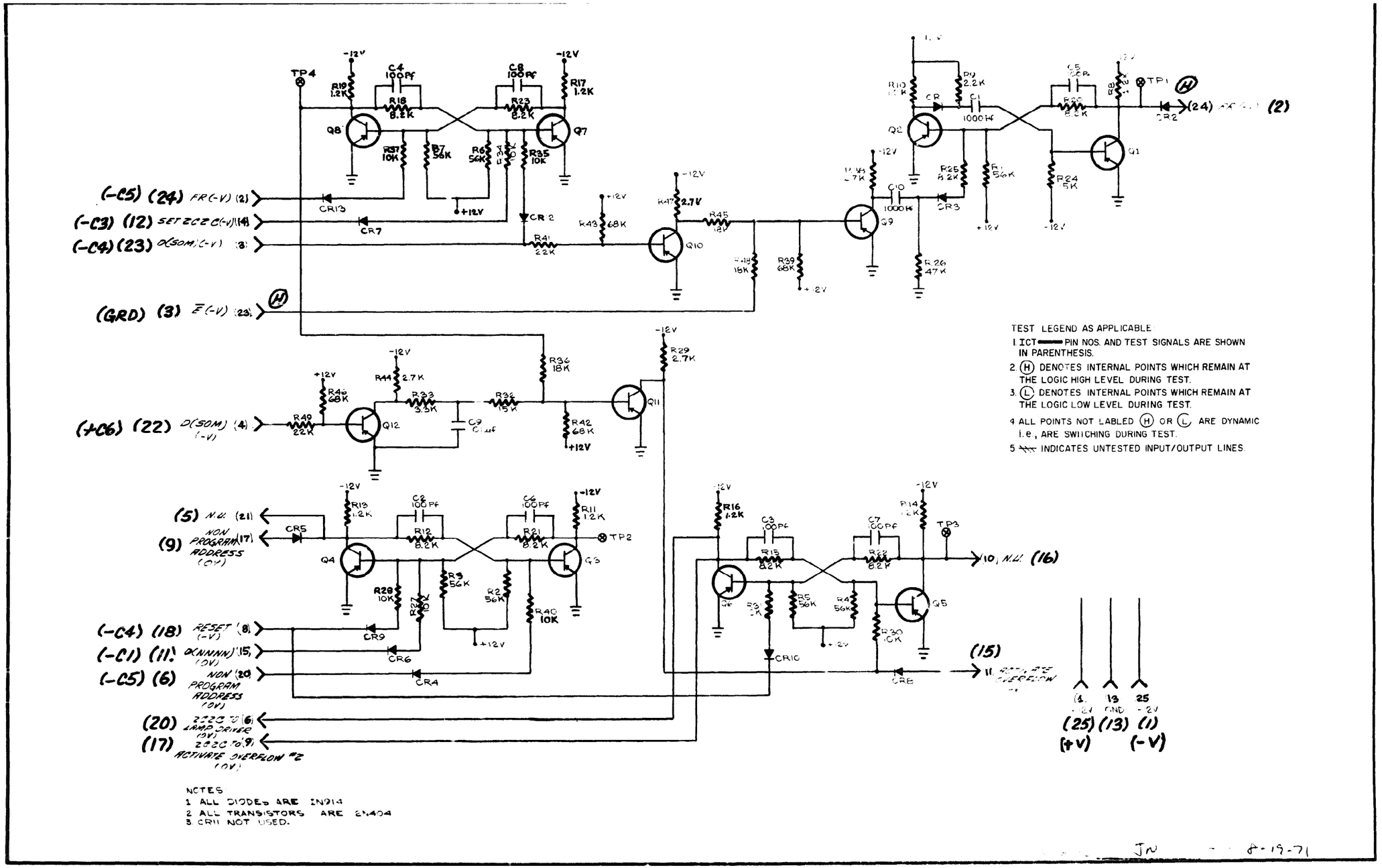
DYNATRONICS TESTAGRAM

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO 4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#"; VALID TEST IS GO INDICATION.
4. NT INDICATES NO TEST.

GOVT APPD. JN DATE 8-19-71



TEST LEGEND AS APPLICABLE

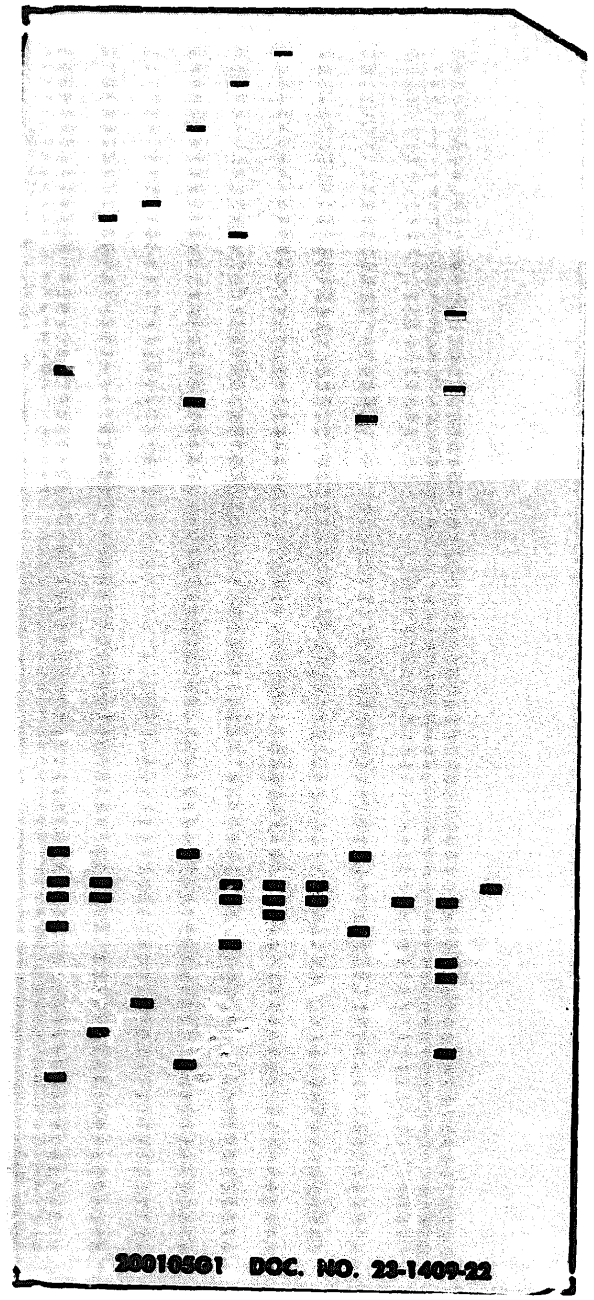
1 ICT ——— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5 ~~~ INDICATES UNTESTED INPUT/OUTPUT LINES.

NOTES
1 ALL DIODES ARE IN914
2 ALL TRANSISTORS ARE 2N404
3 CR11 NOT USED.

JN 8-19-71

P.C. Assembly 200105G1
P.C. Logic NAVSHIPS 0967 216 3010

Doc. No. 23-1409-22



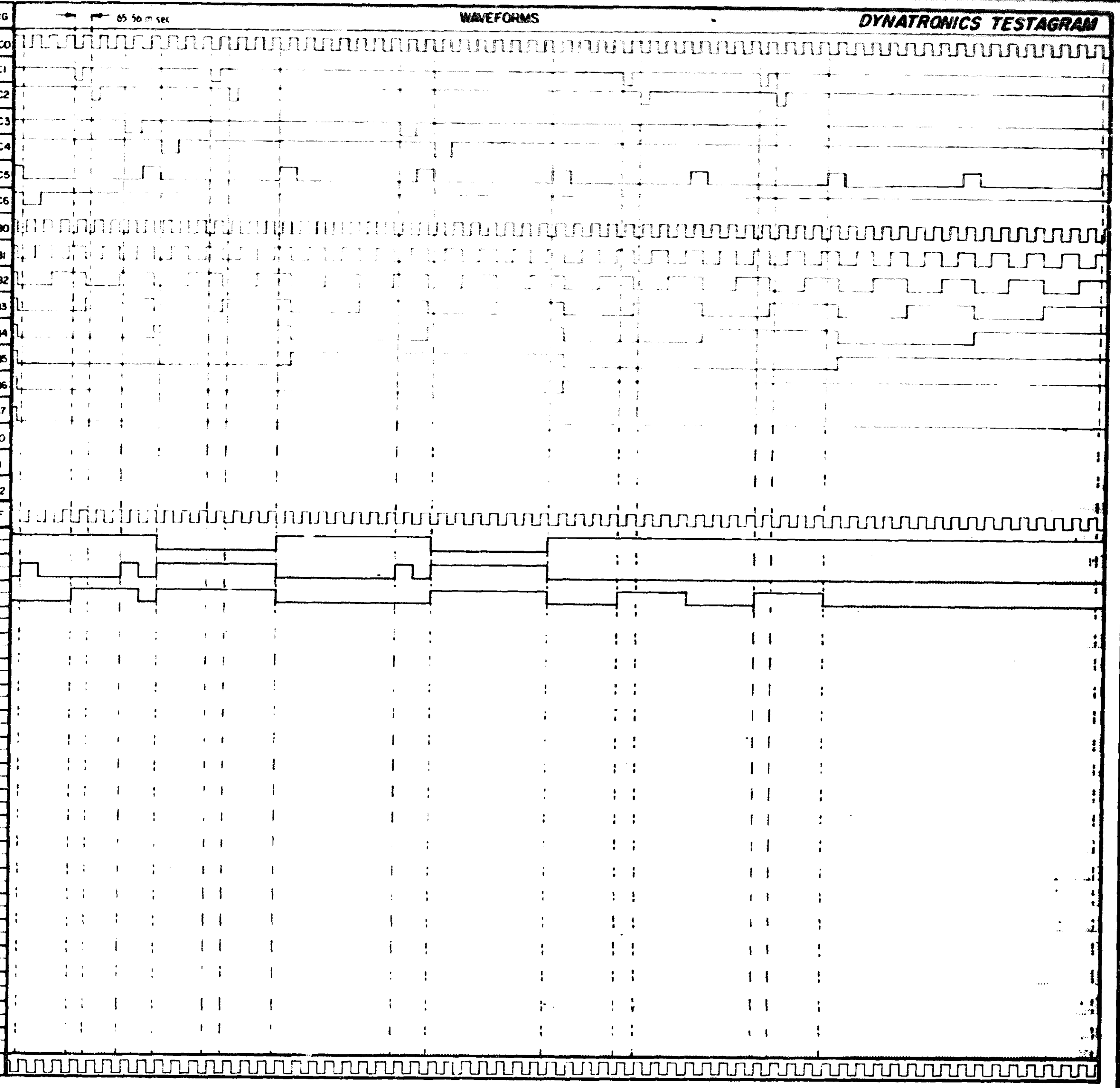
DYNATRONICS TESTAGRAM

TEST PARAMETERS			
V_{cc}	+4.75V	SIG V	GRD, -V
±V	—	LOAD REF V	—
+V	12.0V	CLK	16.39MS
-V	12.0V	BIT CLK	*OSC

ROW ASSIGNMENT	
10	-C4
1	—
2	+V
3	—
4	-V
5	GRD
6	-C5
7	-C1
8	-C3
9	-C6

INPUT PINS	COL	SIG
	63	+C0
11	64	-C1
	65	-C2
12	66	-C3
23, 19	67	-C4
24*, 6*	68	+C5
22*	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+C0 REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTING								
(16) 17*, 20*	A	1	2	3	4				
	B	2	8	11	6				
15	A	1	2	3	4	5	6	7	
	B	3	7	5	9	2	8	3	
5, 9	A	1	2	3	4	5	6	7	8
	B	4	9	2	8	11	6	11	5



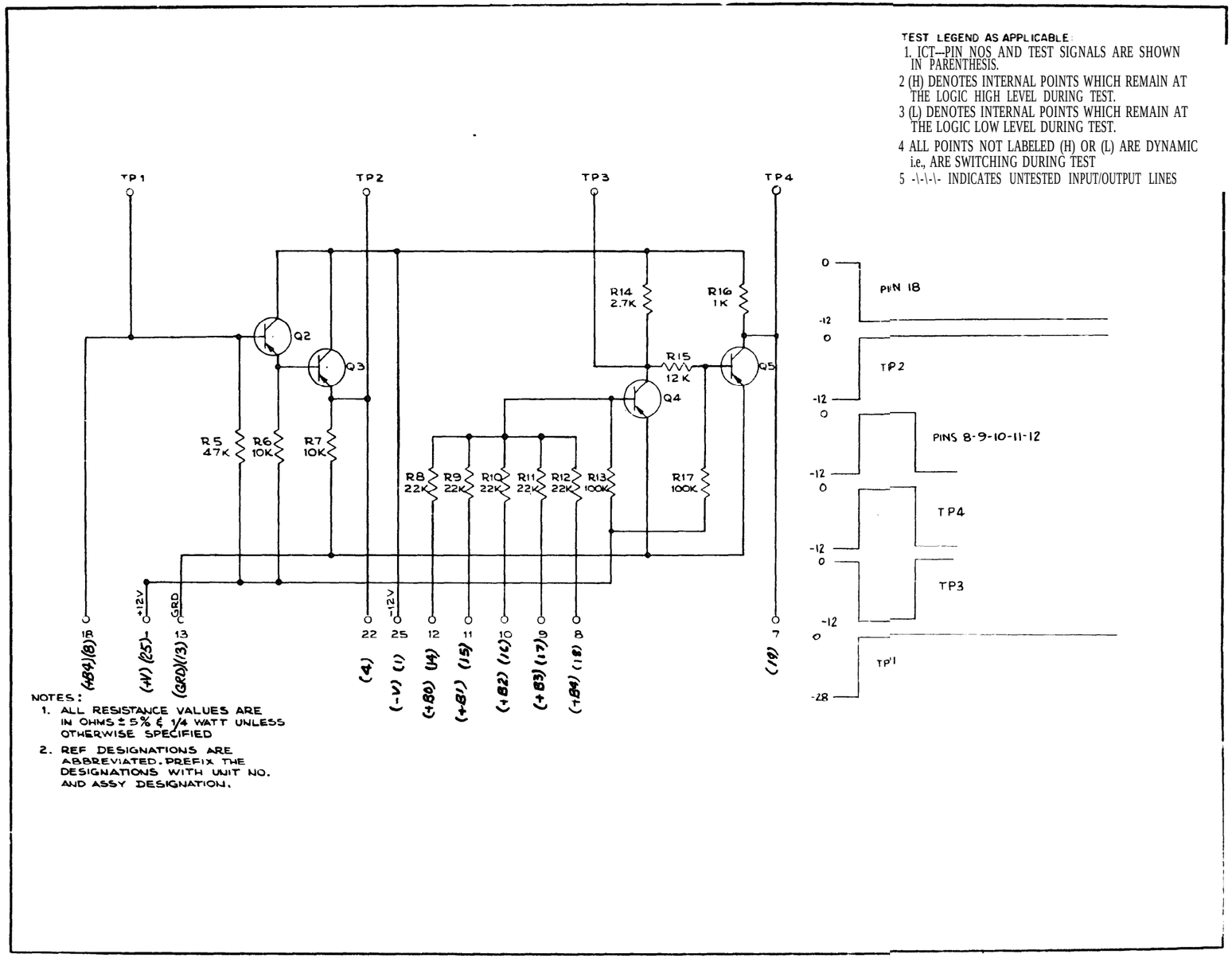
 + BO REF

NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO 4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
4. WAIT SEVERAL SECONDS FOR GO/NO-GO INDICATIONS.

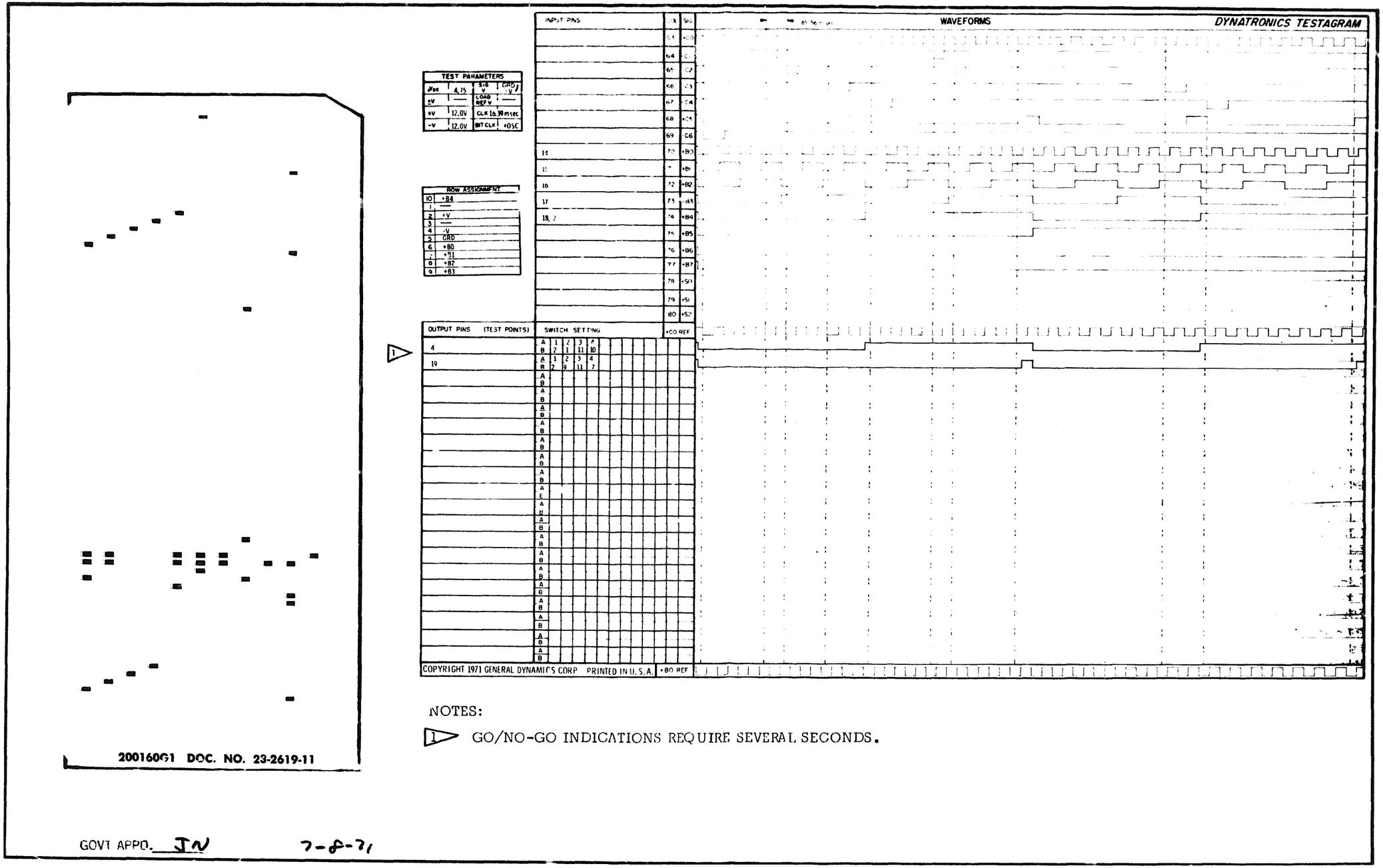
GOVT APPD. JN DATE 8-19-71

Fig. 5-62



P. C. Assembly 200160G1

P.C. Logic NAVSHIPS 0967 216 3010 Doc. No. 230 2619-11
Fig. 5-45



NOTES:

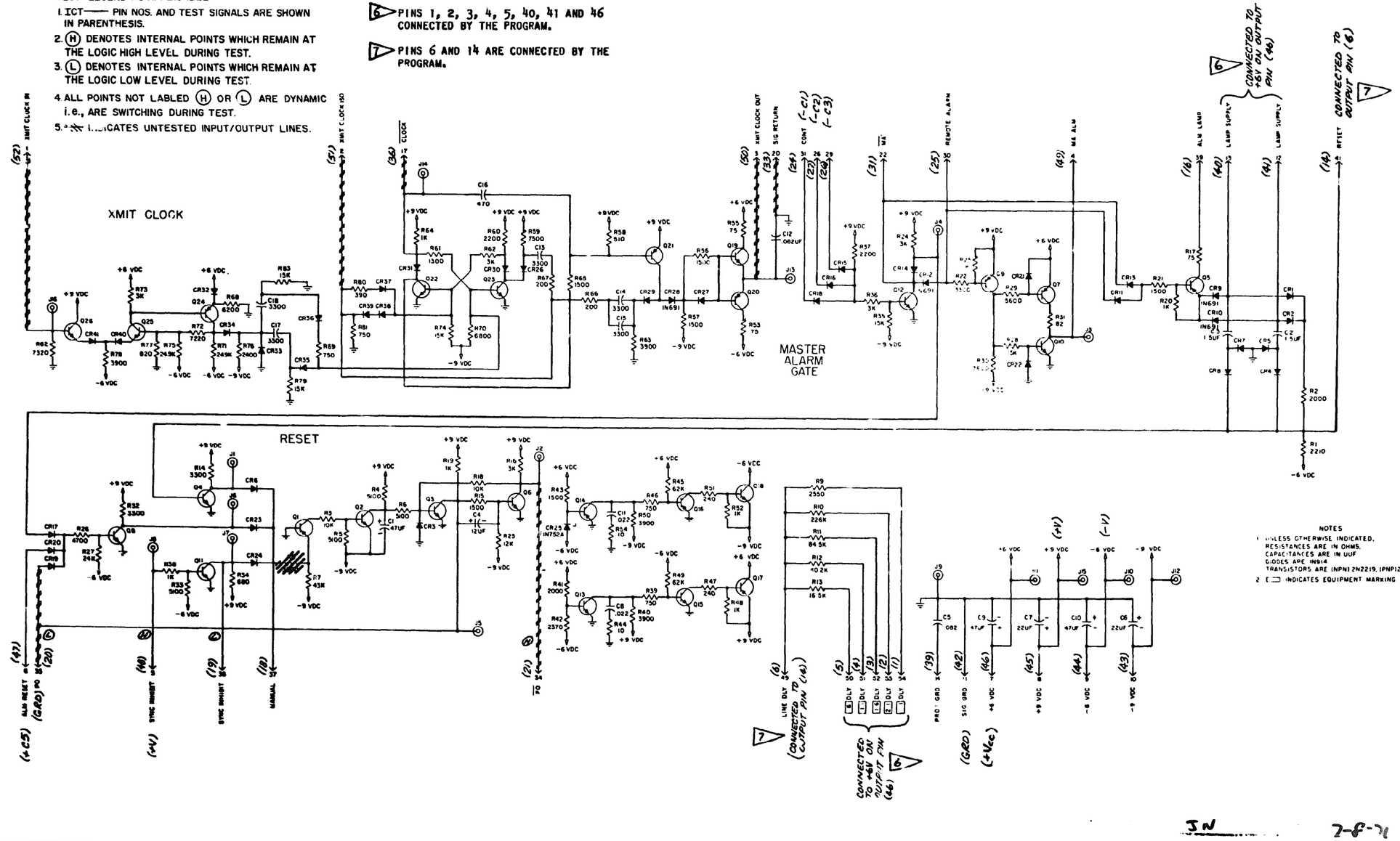
1. GO/NO-GO INDICATIONS REQUIRE SEVERAL SECONDS.

TEST LEGEND AS APPLICABLE:

1. ICT—— PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ~~X~~ INDICATES UNTESTED INPUT/OUTPUT LINES.

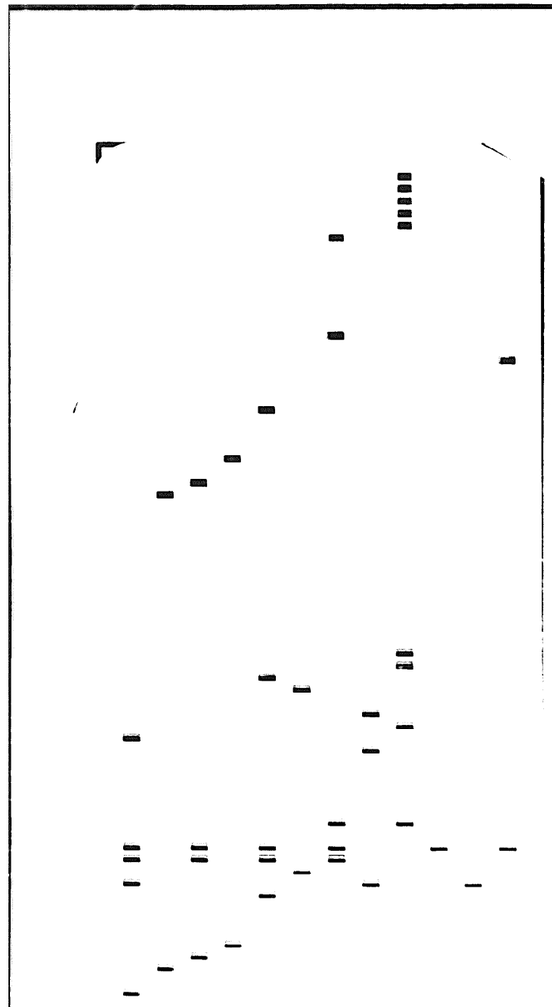
6 PINS 1, 2, 3, 4, 5, 40, 41 AND 46 CONNECTED BY THE PROGRAM.

7 PINS 6 AND 14 ARE CONNECTED BY THE PROGRAM.



P.C. Assembly PL-1120/G (A1)
P.C. Logic TM 5895-543-35-10

Doc. No. 23-2401-11



TEST PARAMETERS			
Vcc	+4.75V	SIG V	GRD +V
±V	—	LOAD REF V	-V
+V	9.0V	CLK	32 µsec
-V	9.0V	BIT CLK	+OSC

ROW ASSIGNMENT	
10	—
1	CONNECTS PINS 1,2,3,4,5 @ 41 and 48
2	+V
3	CONNECTS PINS 6 and 49
4	-V
5	GRD
6	-C1
7	-C2
8	-C3
9	+C5

INPUT PINS	COL	SIG
	63	+CO
24	64	-C1
26	65	-C2
27	66	-C3
	67	-C4
47	68	-C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+CO REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
31, 49, 16*	A: 1 2 3 4 5 6 7 / B: 4 6 8 10 5 9 3
18	A: 1 2 3 4 5 6 7 8 / B: 3 4 6 8 10 5 2 3
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B
	A
	B

+B0 REF

WAVEFORMS — 128 µ sec

DYNATRONICS TESTAGRAM

NOTES:

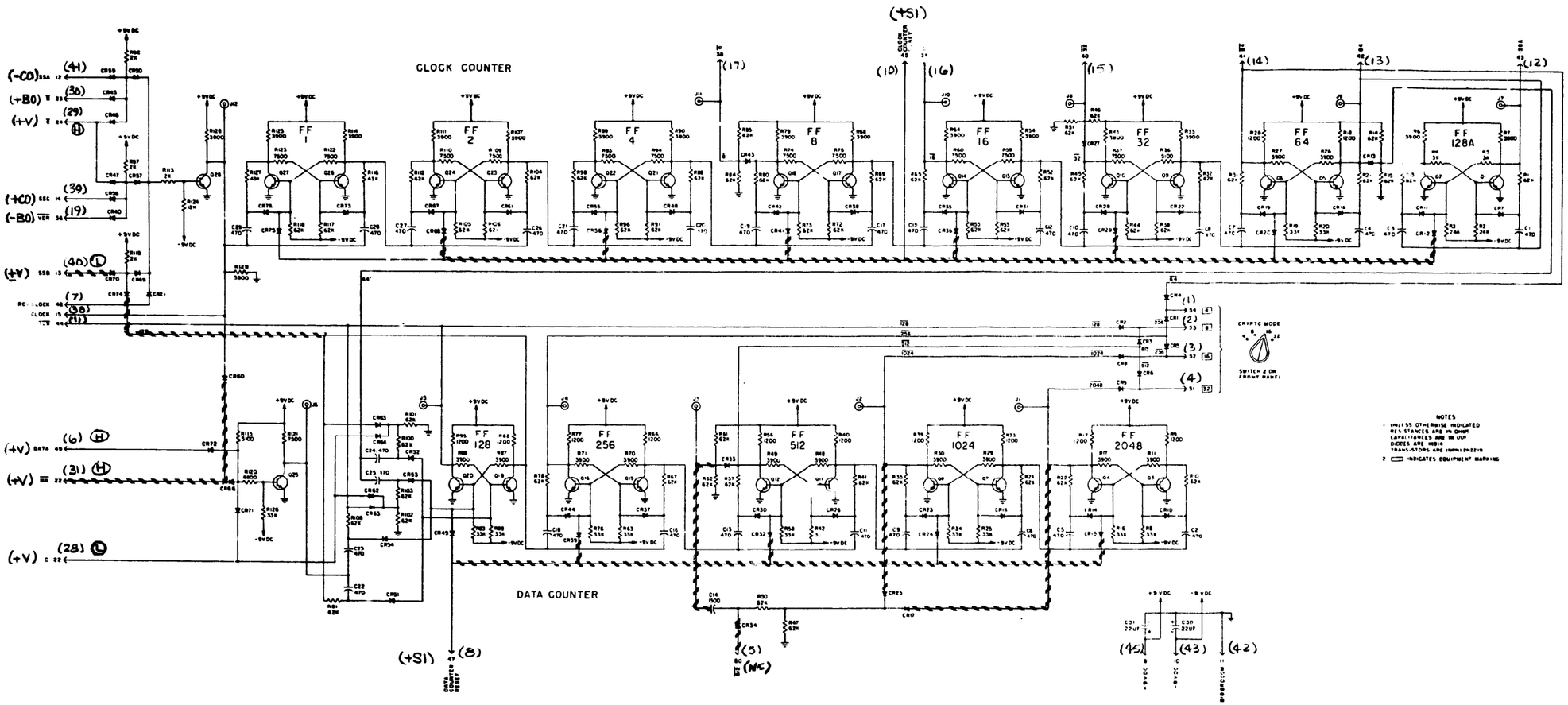
1. * DENOTES INVERTED SIGNAL.

A-1(PL-1120/G) DOC. NO. 23-2401-11

JN 7-8-71

TEST LEGEND AS APPLICABLE

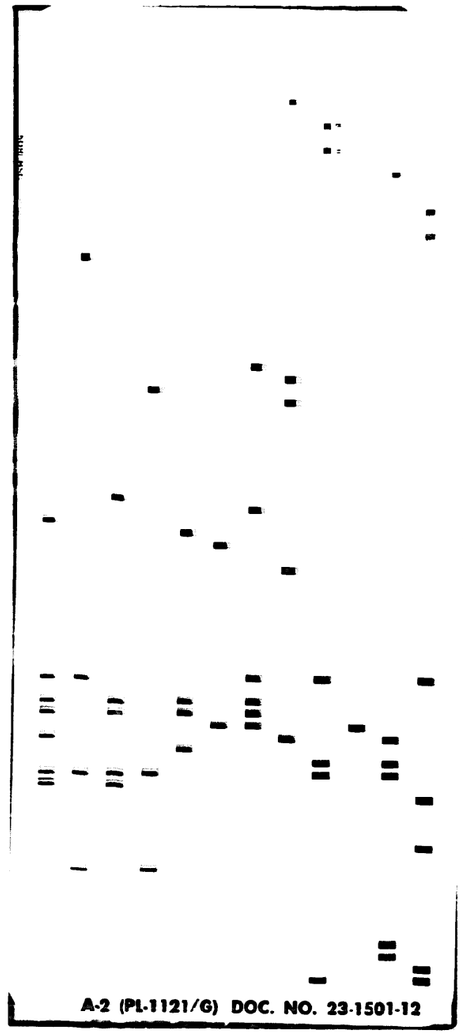
1. ICT------ PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ⚡ INDICATES UNTESTED INPUT/OUTPUT LINES.



APPD. JN DATE 7-8-71

P.C. Assembly PL1121/G
P . C . L o g i c A 2

Doc. No. 23-1501-12



A-2 (PL-1121/G) DOC. NO. 23-1501-12

JN 7-8-71

TEST PARAMETERS			
Vcc	+4.75	SIG V	0 TO +9V
-V	-2V	LOAD REF V	VCC
+V	+9V	CLK	32 u sec
-V	-9V	BIT CLK	÷OSC

ROW ASSIGNMENT	
10	—
1	+S1
2	+V
3	+V
4	-V
5	GND
6	+B0
7	+C0
8	-B0
9	-C0

INPUT PINS	COL	SIG
41, 39	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
30, 19*	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
10, 8	79	+S1
	80	+S2
		+C0 REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
38	A 1 2 3 / B 2 3 4
17	A 1 2 / B 8 2
16	A 1 2 / B 2 1
15	A 1 2 3 4 5 6 7 / B 1 10 NT NT NT 2 #
13, 14*	A 1 2 3 4 / B 10 6 NT 8
⑫ ⑪	A 1 2 / B 6 8
Q26 (REF)	A / B
Q23 (REF)	A / B
Q21 (REF)	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B
	A / B

WAVEFORMS — DYNATRONICS TESTAGRAM

← → 128 u sec

]

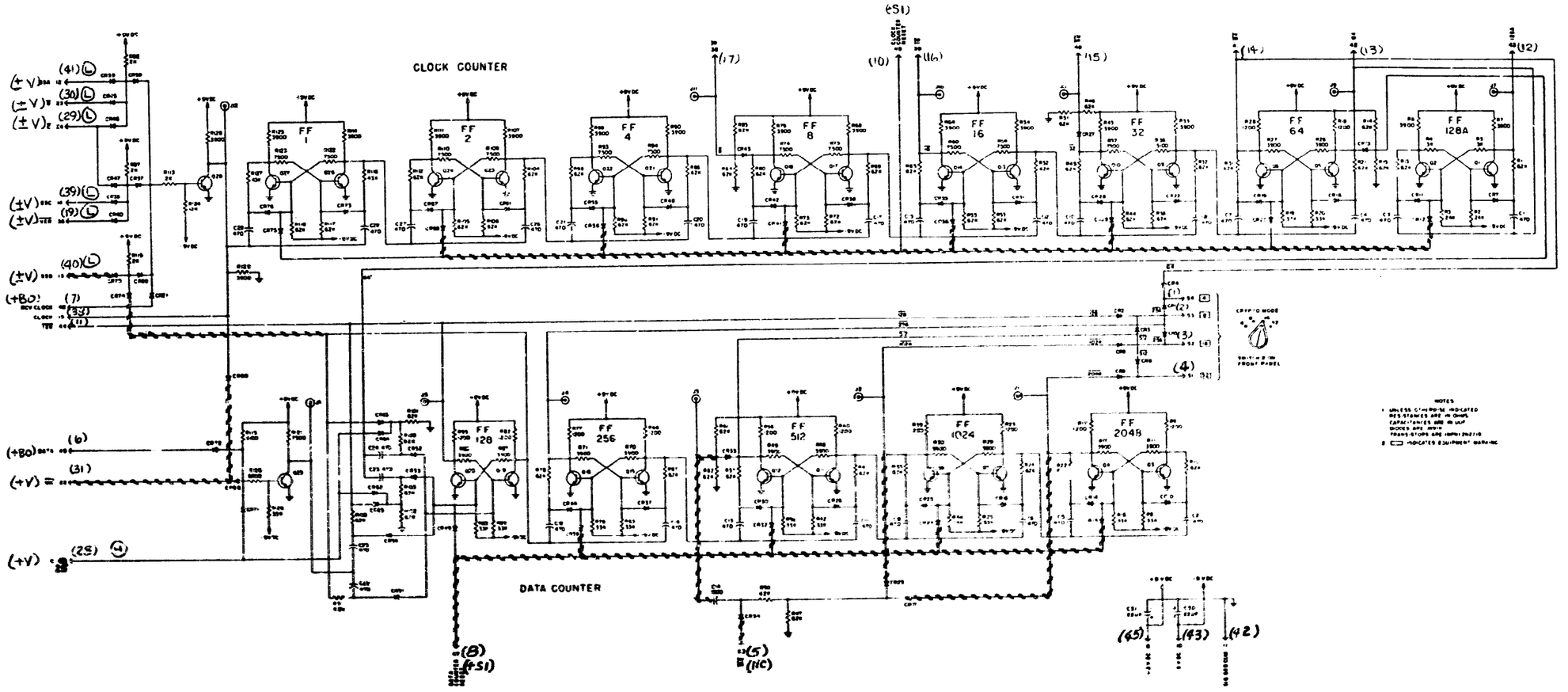
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. IN ICT-102 TESTER "#" DENOTES ALL POSITIONS OF "B" SWITCH ARE NO-GO FOR VALID TEST.

   IN ICT-103 TESTER PRESS "B" SWITCH "#" WHERE INDICATED BY "#" ; VALID TEST IS GO INDICATION.
4. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.
5. NT INDICATES NO TEST.

TEST LEGEND AS APPLICABLE:

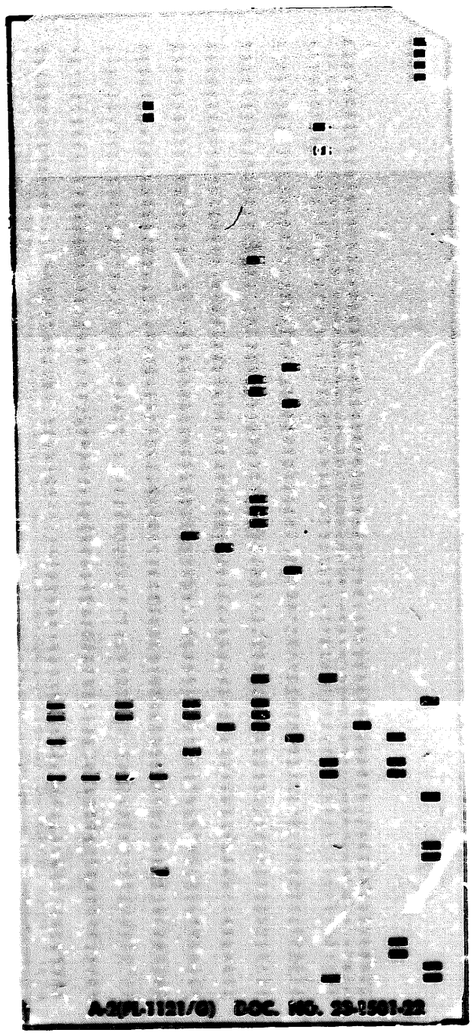
1. IC† ----- PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST
5. ⇝ INDICATES UNTESTED INPUT/OUTPUT LINES



JN 7-8-71

P.C. Assembly PL 1121/G
P.C. Logic A2

Doc. No. 23-1501-22



A2(PL1121/G) DOC. NO. 23-1501-22

DYNATRONICS TESTAGRAM

WAVEFORMS

← → 128 μ sec

TEST PARAMETERS			
Vcc	+4.75V	SIG V	-2 TO +9V
±V	-2V	LOAD REF V	GRD
+V	+9V	CLK	32 U SEC
-V	-9V	BIT CLK	+0.2C

ROW ASSIGNMENT	
10	—
1	+S1
2	+V
3	±V
4	-V
5	GRD
6	+B0
7	—
8	—
9	—

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
7, 6	70	+B0
	71	+B1
	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
8, 10	79	+S1
	80	+S2
		+C0 REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
38	
11	
①	
②	
③	
④	
015 (REF)	
011 (REF)	
07 (REF)	
03 (REF)	
09 (REF)	
05 (REF)	

+B0 REF

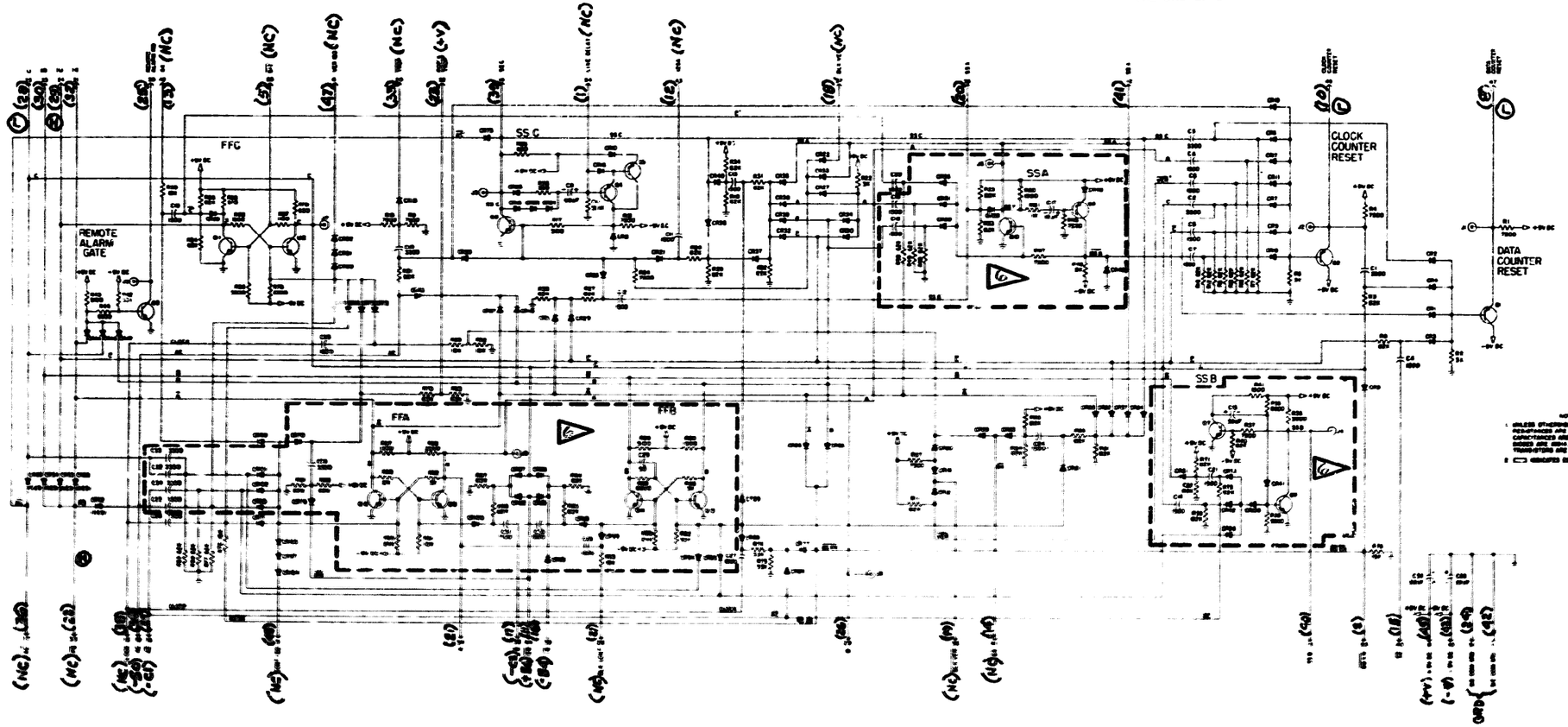
NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

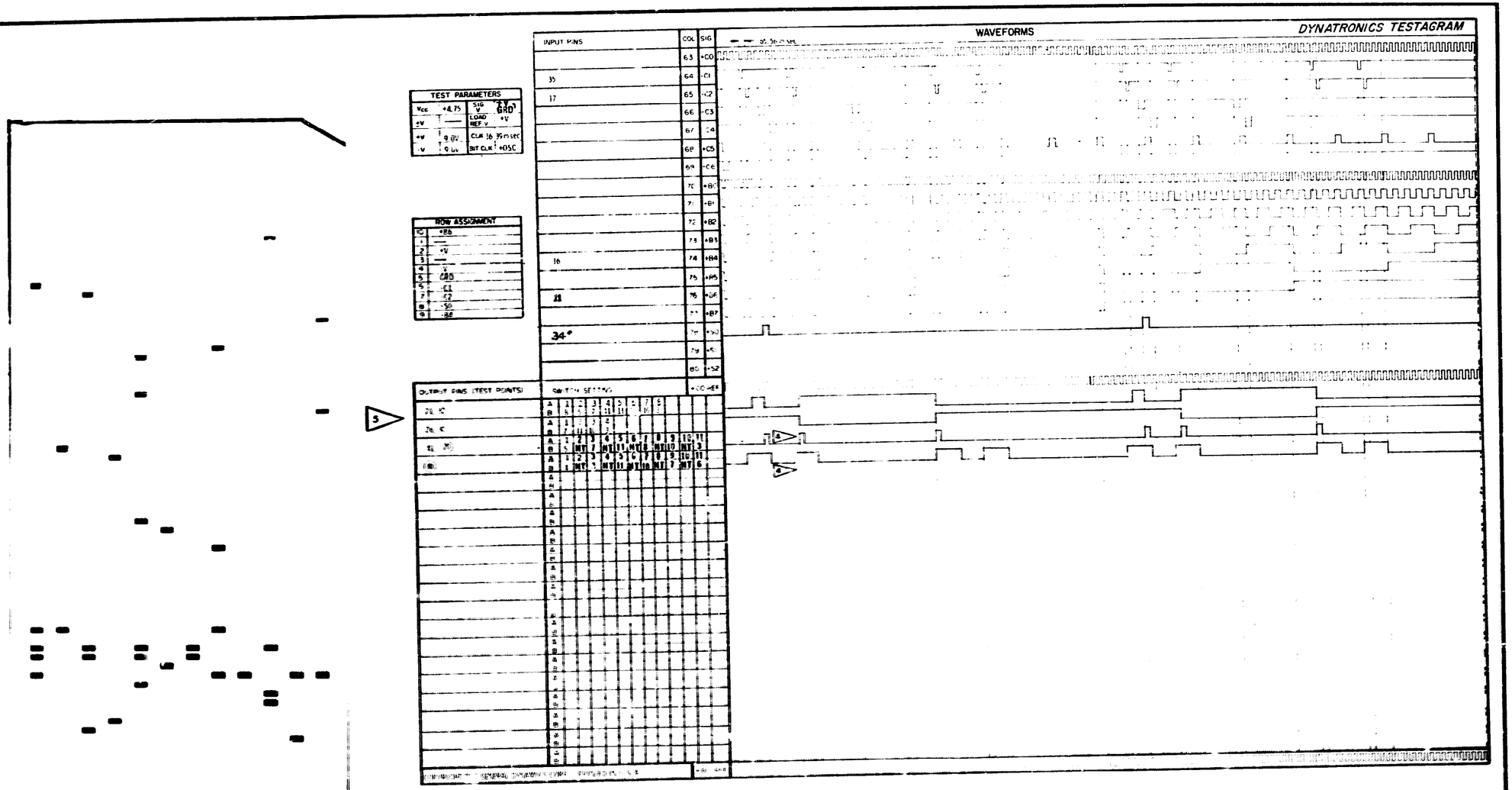
GOVT APPD. JW DATE 2-5-71

TEST LEGEND AS APPLICABLE:

1. ICT——● PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ⋘ INDICATES UNTESTED INPUT/OUTPUT LINES.
6. THIS CARD IS PARTIAL TESTED. THE AREAS WITHIN THE DASHED LINES ARE GO/NO-GO TESTED.



P.C. Assembly PL-1122/G
P.C. Logic TM 5895-543-35-12 Doc. No. 23-2402-11



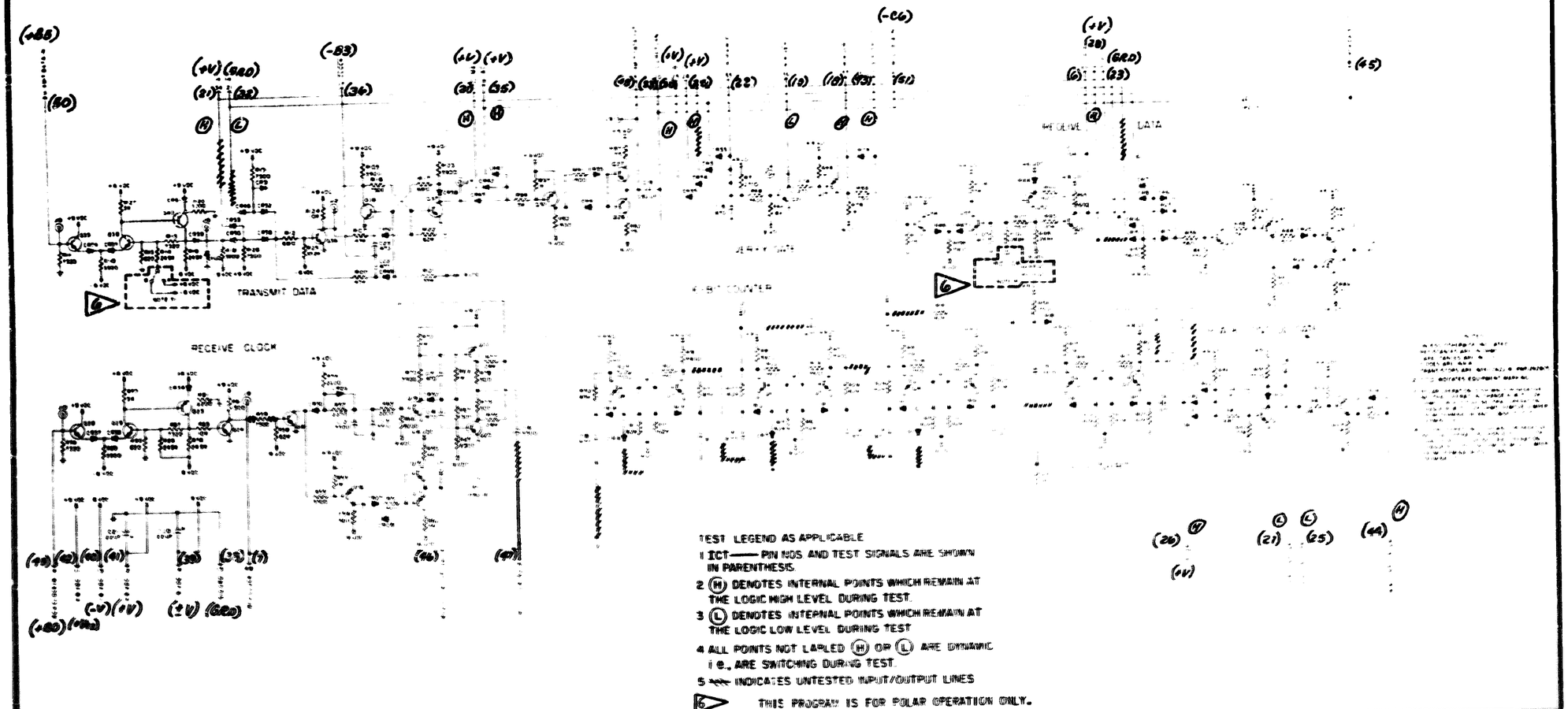
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

1 ONLY THE LEADING EDGES ARE TESTED BECAUSE OF THE VARIATIONS IN ONE SHOT "ON" TIME.

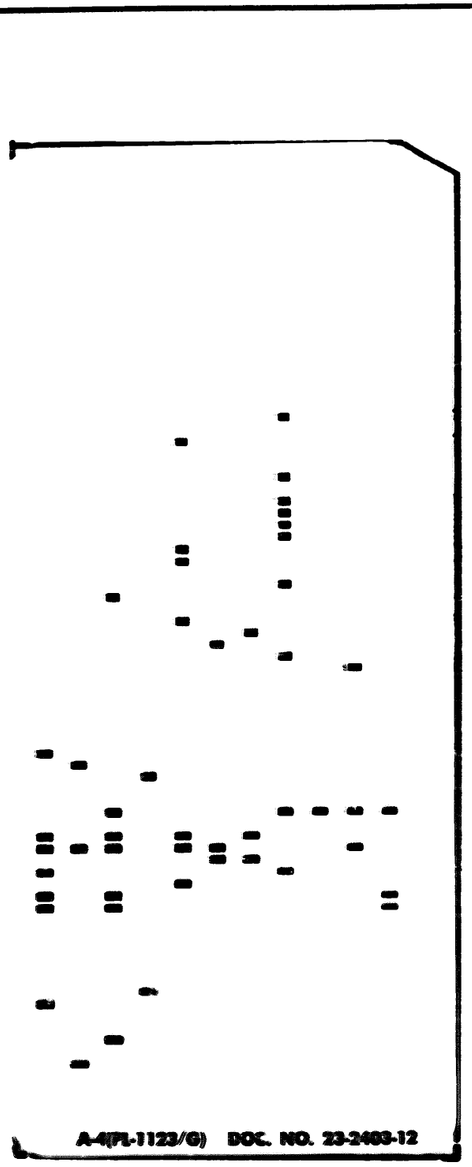
5 GO/NO-GO INDICATIONS REQUIRE SEVERAL SECONDS.

6. NT INDICATES NO TEST.

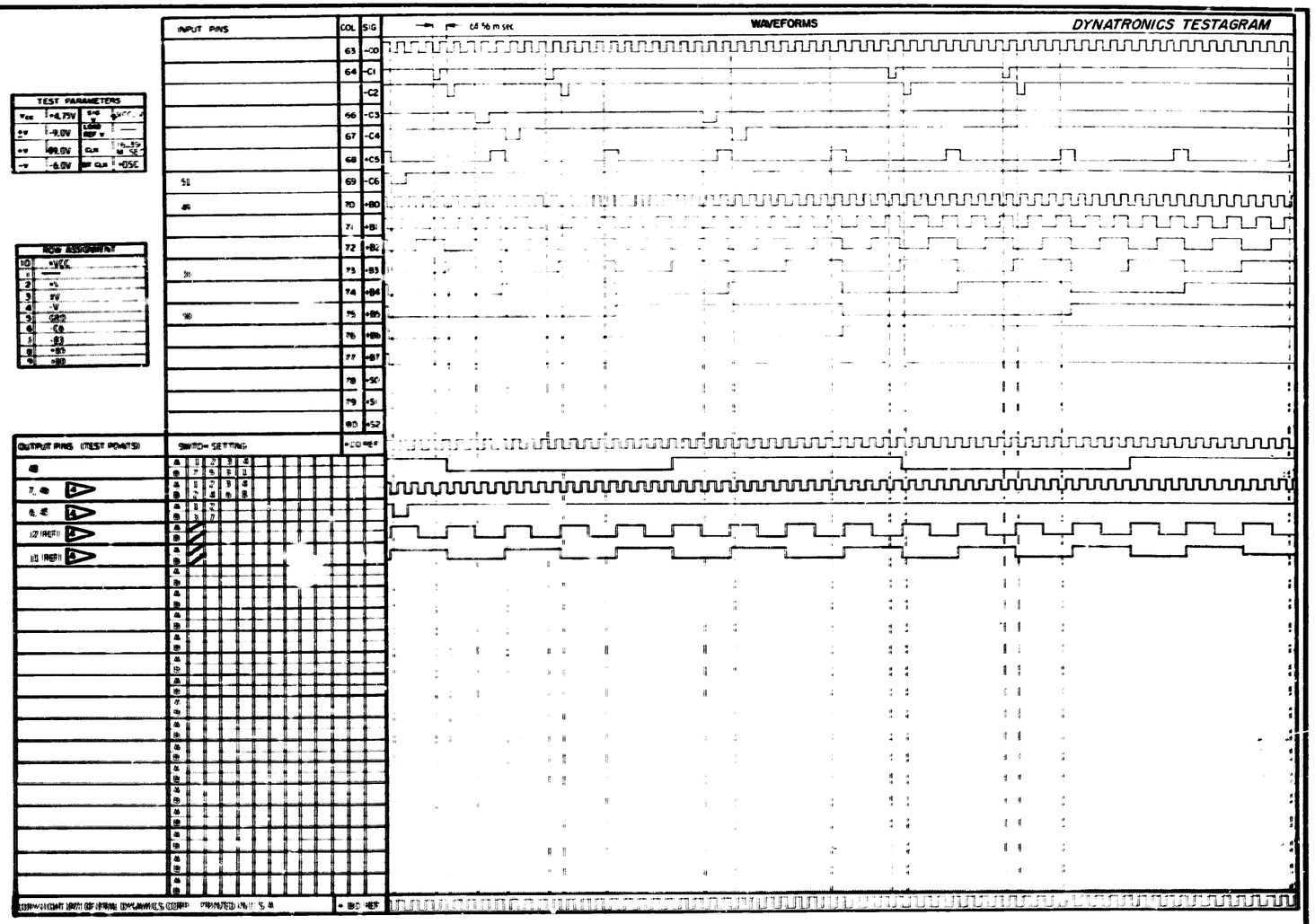


GOVT APPD. _____ DATE 7-16-71

P.C. Assembly PL-1123
P.C. Logic TM 5895-543-35-13 Doc. No. 23-2403-12

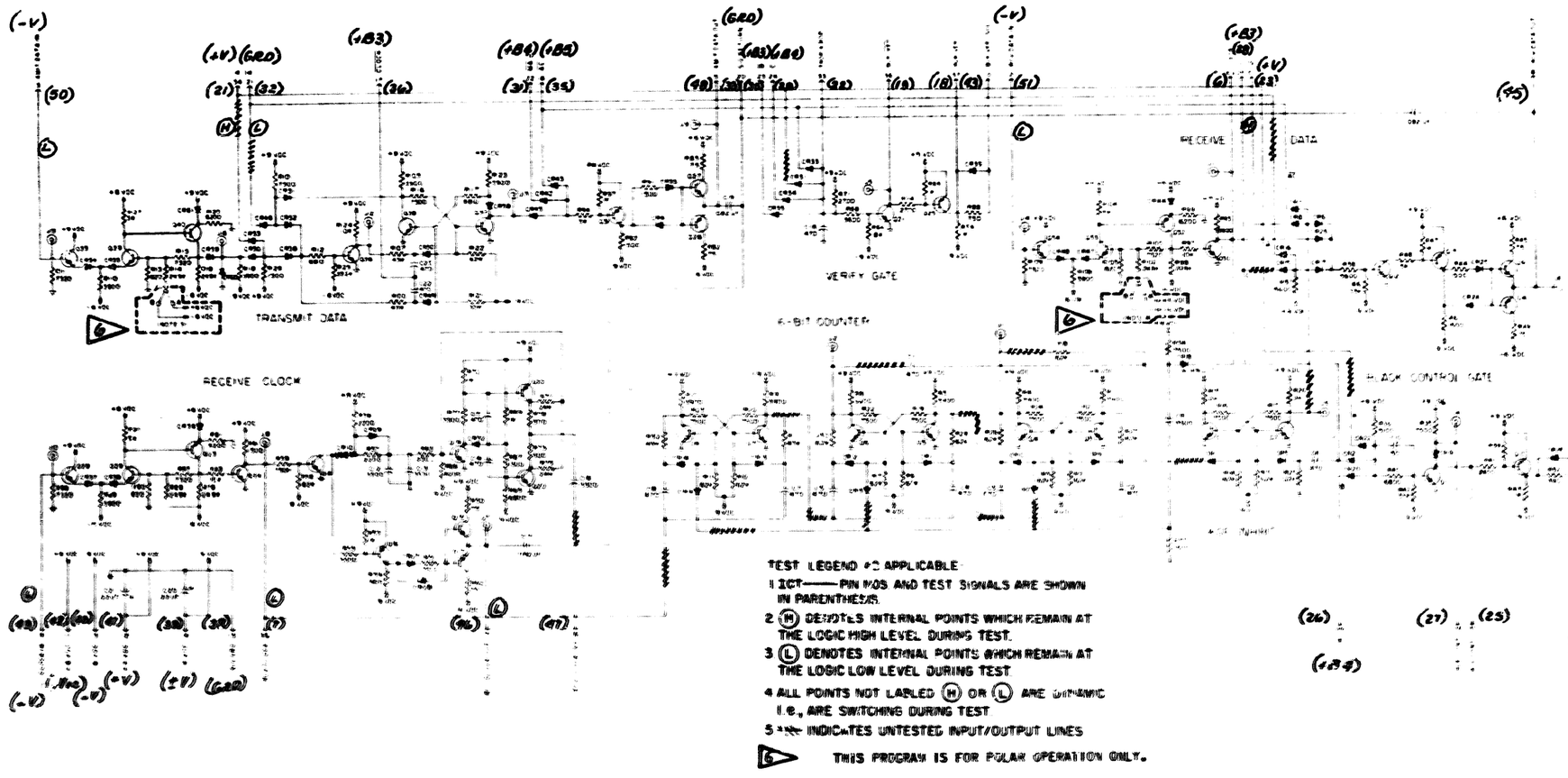


A-4(PL-1123/G) DOC. NO. 23-2403-12



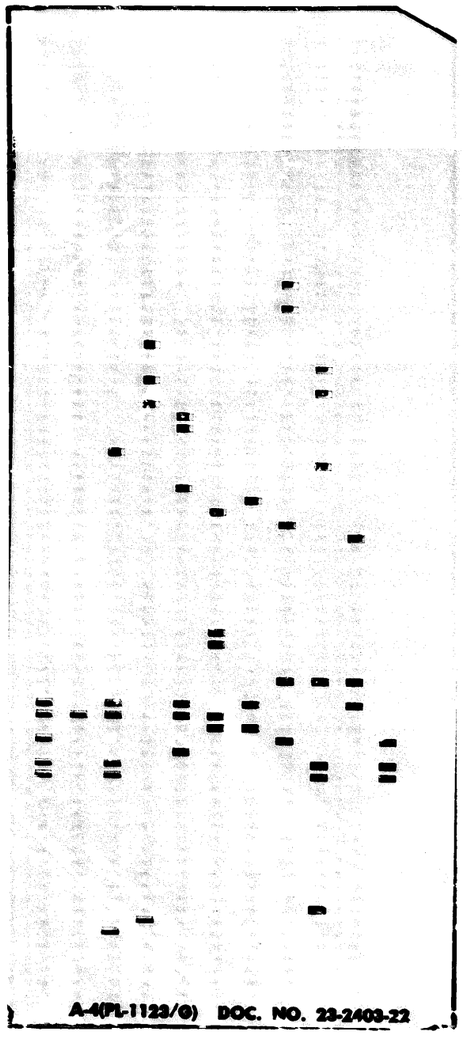
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5ENT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. THIS PROGRAM IS FOR POLAR INPUT OPERATION ONLY.
4. OUTPUT PINS 6, 7, J1 AND J2 HAVE A SIGNAL LEVEL OF +6V TO GRD. ALL OTHER OUTPUTS ARE VCC TO -V (+5V TO -6V).
5. WAIT SEVERAL SECONDS FOR GO/NO-GO INDICATIONS.



GOVT APPD. _____ DATE _____

P.C. Assembly PL-1123
P.C. Logic TM 5895-543-35-13 Doc. No. 23-2403-22



A-4(PL-1123/0) DOC. NO. 23-2403-22

TEST PARAMETER

Vcc	+4.75V	SIG	
+V	+5.0V	+CO(n) REF V	
+V	+9.00V	CLR	MASTER CLR
-V	-5.0V	INIT CLR	+OSC

ROW ASSIGNMENT

10	+VCC
	+B3
2	+V
3	+V
4	-V
5	GRD
6	+B4
7	+B5
8	—
9	—

INPUT PINS	COL	SIG
	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
36, 30, 28	73	+B3
31, 29, 26	74	+B4
35	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+CO REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
48 [4]	A 1 2 3 4 / B 2 10 9 6
18, 43, 22, 19 [5] [6] [7]	A 1 2 3 4 / B 2 8 8 11
45 [4]	A 1 2 3 4 / B 2 11 9 7
44, 25*, 27* [5] [6] [7]	A 1 2 3 4 5 / B 2 6 11 4 6

WAVEFORMS — 65.5m sec

DYNATRONICS TESTAGRAM

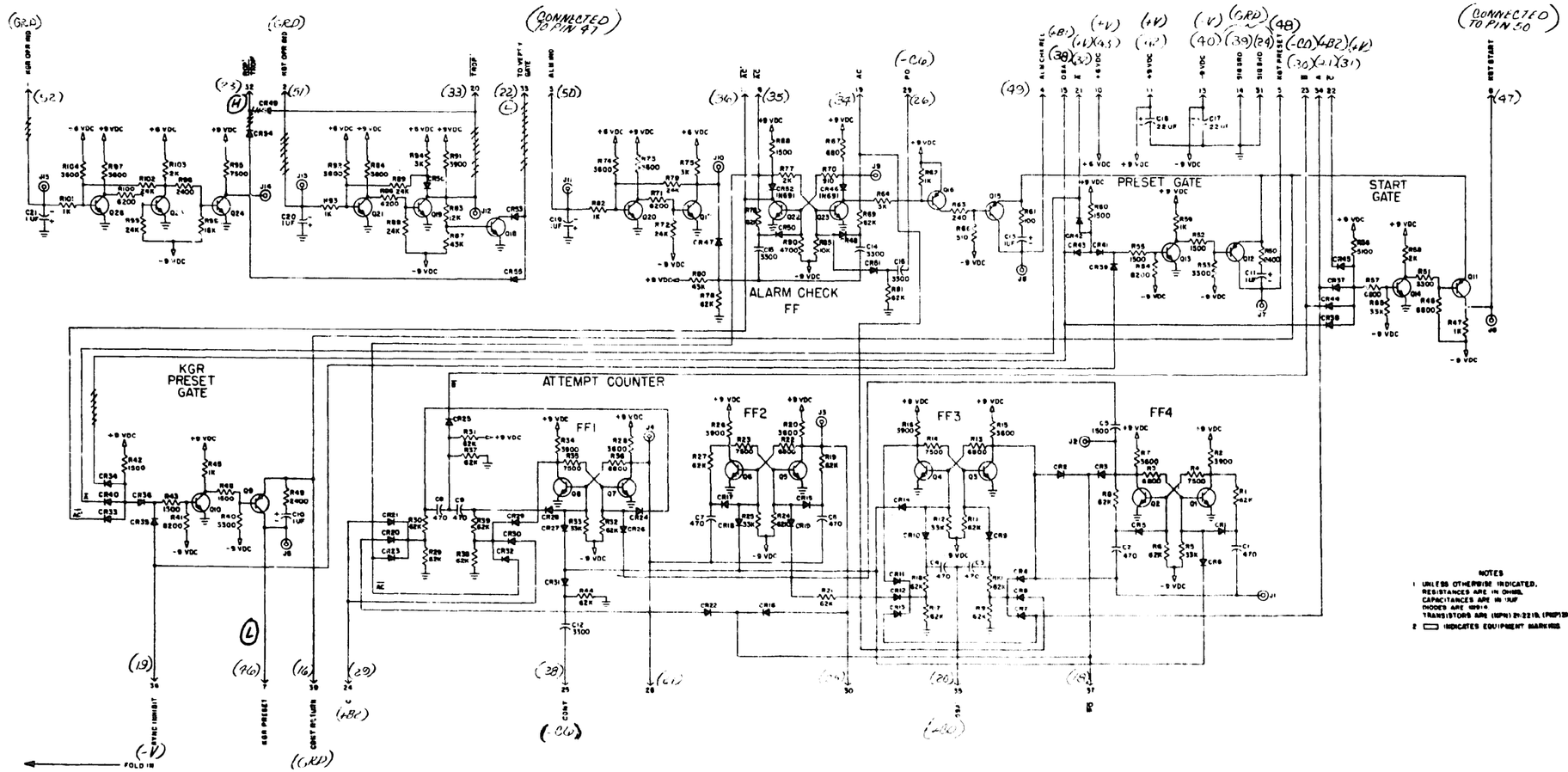
NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO 4.75V.
3. THIS PROGRAM IS FOR POLAR OPERATION ONLY.
4. SIGNAL LEVEL IS VCC TO -V (5V TO -9V).
5. PINS 18,43 AND 44 HAVE SIGNAL LEVELS OF +V TO ±V (+9V TO -9V).
6. PINS 19 AND 25 ARE +7V TO GRD SIGNAL LEVELS.
7. PINS 22 AND 27 ARE VCC TO GRD SIGNAL LEVELS (+5V TO GRD).
8. WAIT SEVERAL SECONDS FOR GO/NO-GO INDICATIONS.

GOVT APPD. JN DATE [illegible]

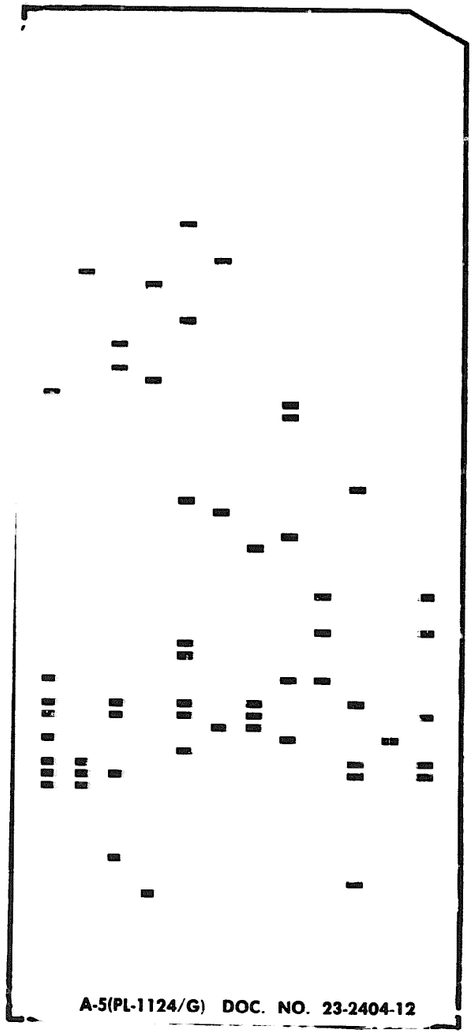
TEST LEGEND AS APPLICABLE

1 ICT——PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2 (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3 (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4 ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5 ⚡ INDICATES UNTESTED INPUT/OUTPUT LINES



P.C. Assembly PL-1124/G
P.C. Logic TM 5895-543-35-14

Doc. No. 23-2404-12



A-5(PL-1124/G) DOC. NO. 23-2404-12

TEST PARAMETERS			
V_{cc}	+4.75V	0 to LOAD REF V	+V, GRD
±v	+6.0V		-V
+v	9.0V	CLK	16.39 M. Sec.
-v	9.0V	BIT CLR	+OSC

ROW ASSIGNMENT	
10	+B1
1	CONNECT PINS 47 and 30
2	+V
3	±V
4	-V
5	GRD
6	+B2
7	-C6
8	+C0
9	-C0

INPUT PINS	COL	SIG
20, 30*	63	+C0
	64	-C1
	65	-C2
	66	-C3
	67	-C4
	68	+C5
26, 28	69	-C6
	70	+B0
38	71	+B1
21, 29	72	+B2
	73	+B3
	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	+S0
	79	+S1
	80	+S2
		+C0 REF

WAVEFORMS — 65.56 m sec — DYNATRONICS TESTAGRAM

5

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
34, 35*, 36*	A 1 2 3 4 5 / B 6 11 2 10 4
27	A 1 2 3 4 5 6 7 8 / B 3 9 9 4 8 11 3 7
25	A 1 2 3 4 / B 3 9 8 11 3 2
(18) 4	A 1 2 3 4 / B 3 5 3 7

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NOTES:

1. * DENOTES INVERTED SIGNAL.
2. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
3. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

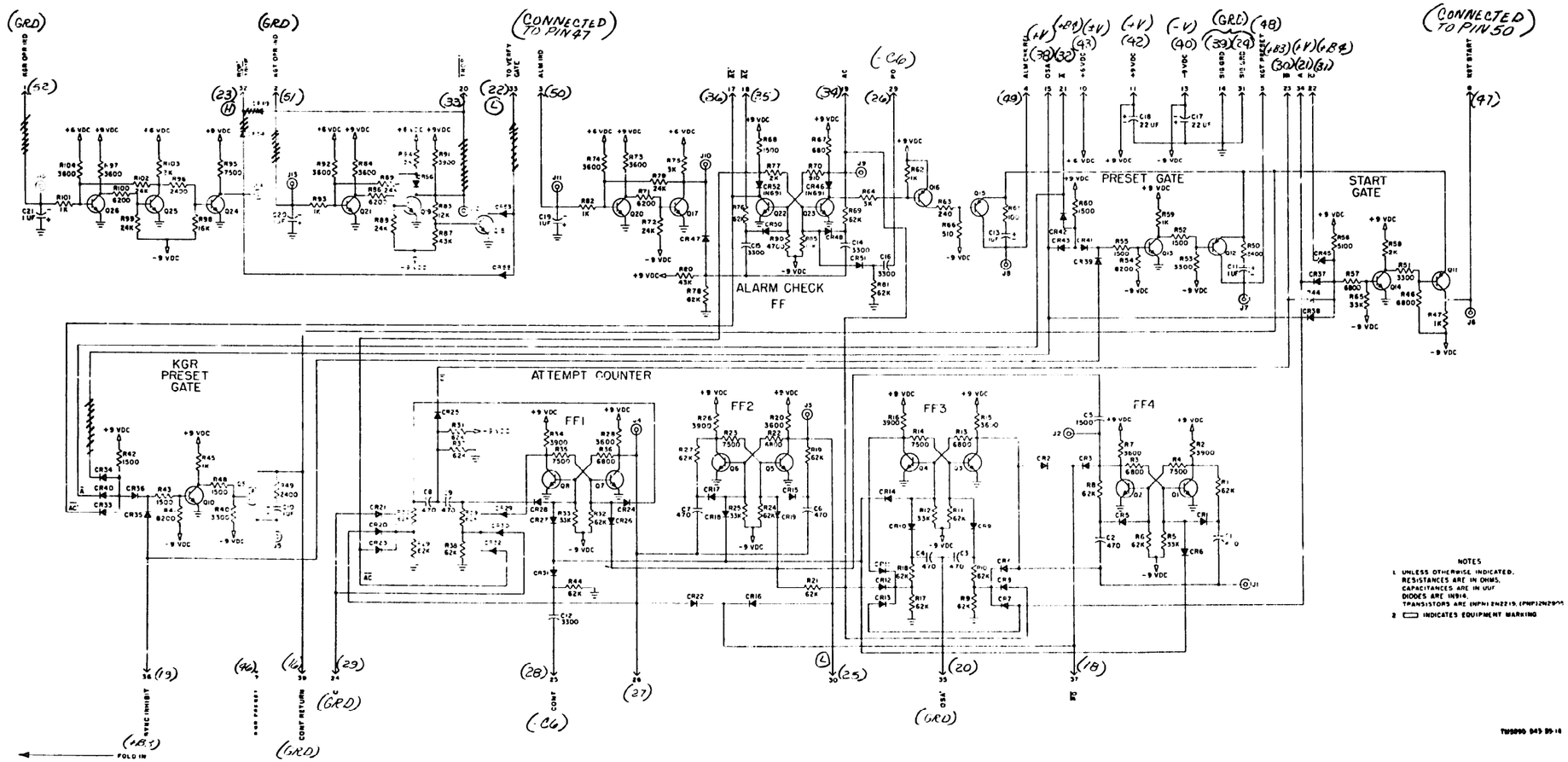
4 DUE TO LOADING FACTORS THE OUTPUT ON PIN (18) CAN ONLY BE OBSERVED WHEN PIN (18) IS SELECTED ON THE IN/OUT SELECTOR SWITCHES.

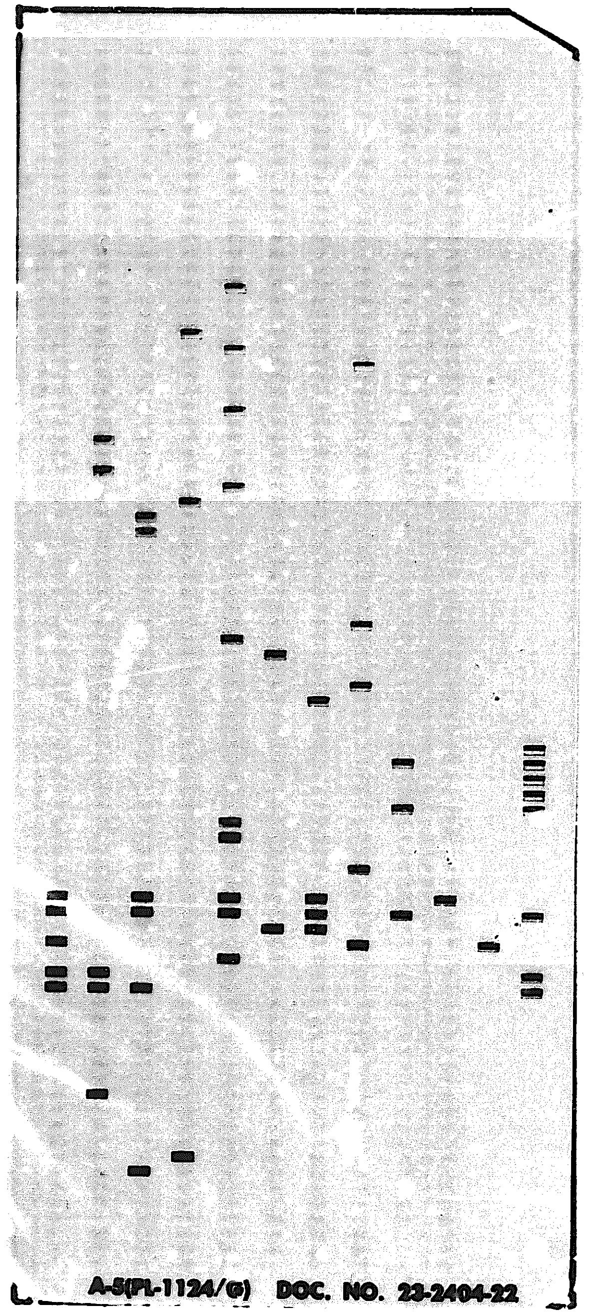
5 GO/NO-GO INDICATIONS REQUIRE SEVERAL SECONDS.

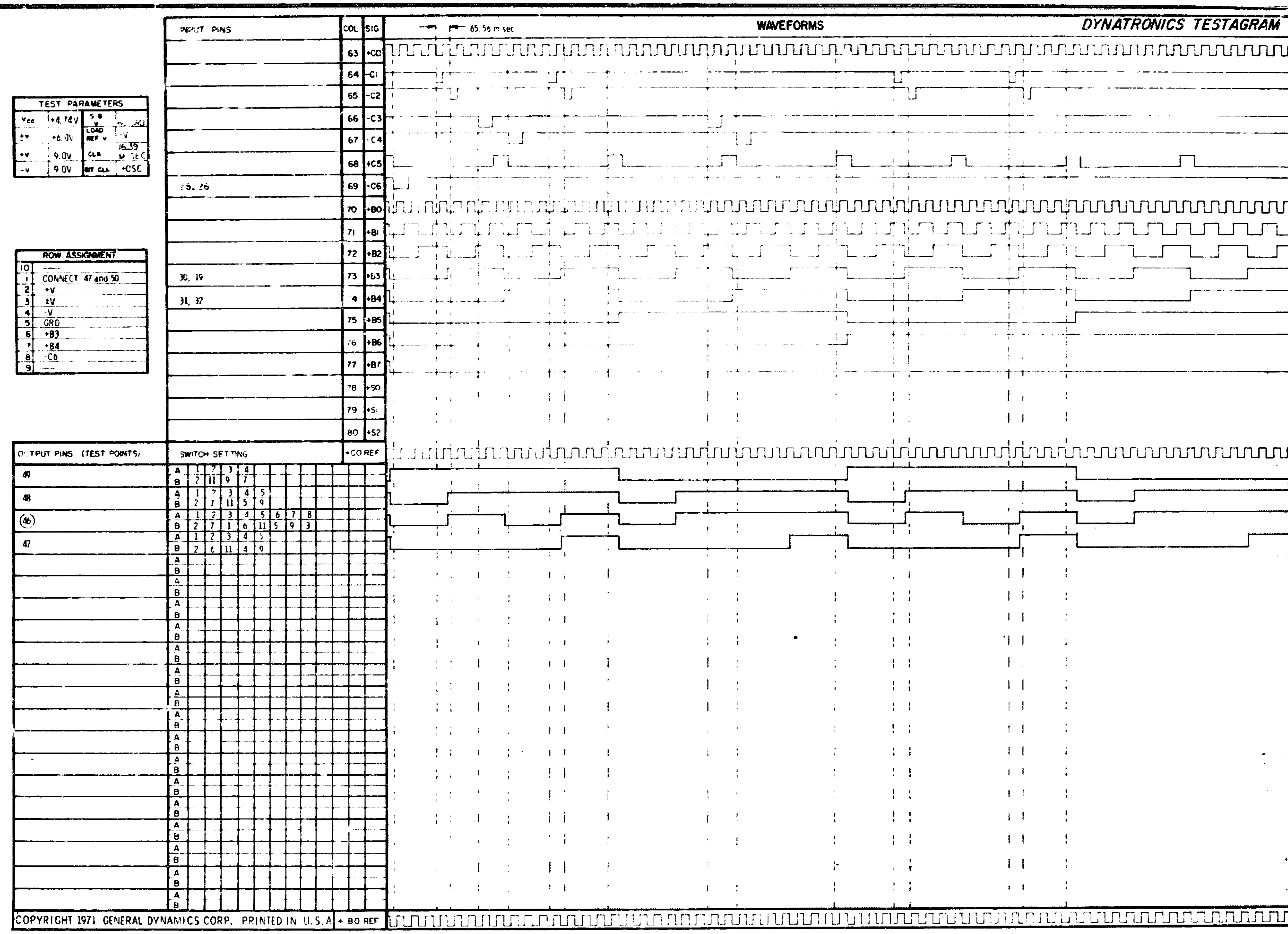
APPROVED JN DATE 7-9-71

TEST LEGEND AS APPLICABLE:

1. ICT——PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.
3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.
4. ALL POINTS NOT LABLED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.
5. ⟿ INDICATES UNTESTED INPUT/OUTPUT LINES.







NOTES:

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.

2. ENCIRCLED OUTPUT PINS ARE "KEY" AND SHOULD BE GO/NO-GO TESTED FIRST.

3▷ GO/NO-GO INDICATIONS REQUIRE SEVERAL SECONDS.

JN 7-9-71

TEST LEGEND AS APPLICABLE

1 ICT-PIN NOS. AND TEST SIGNALS ARE SHOWN IN PARENTHESIS.

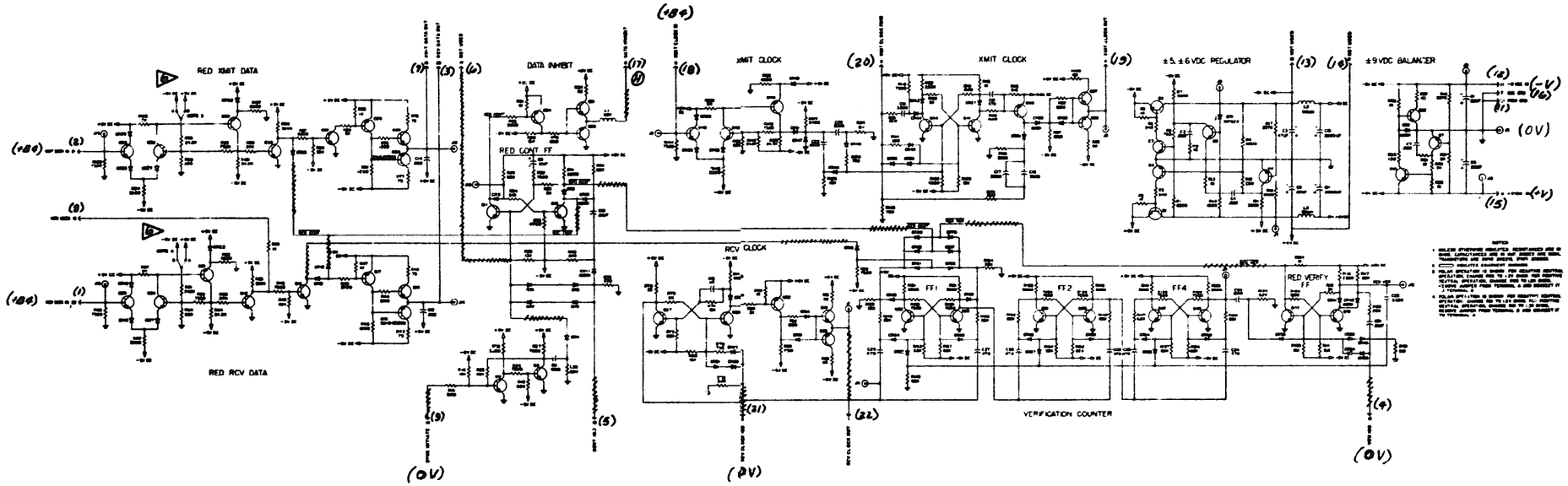
2. (H) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC HIGH LEVEL DURING TEST.

3. (L) DENOTES INTERNAL POINTS WHICH REMAIN AT THE LOGIC LOW LEVEL DURING TEST.

4 ALL POINTS NOT LABELED (H) OR (L) ARE DYNAMIC i.e., ARE SWITCHING DURING TEST.

INDICATES UNTESTED INPUT/OUTPUT LINES.

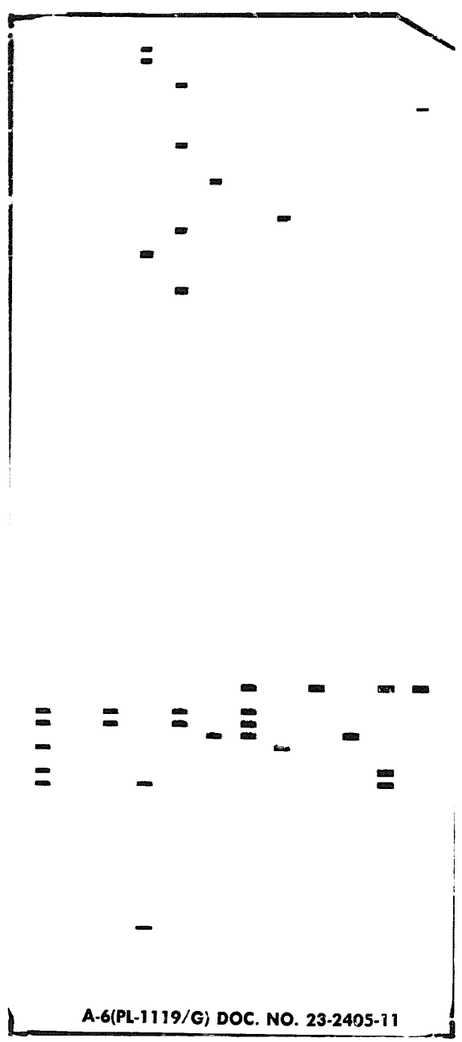
THIS PROGRAM IS FOR POLAR INPUT OPERATION ONLY.



COMP APPD. JN DATE 2-15-77

P.C. Assembly PL-1119/G
P.C. Logic TM 5895-543-35-15

Doc. No. 23-2405-11



A-6(PL-1119/G) DOC. NO. 23-2405-11

TEST PARAMETERS			
V_{EO}	+4.75V	SIG V (LOGIC REF V)	+V_{CC} EXT
-V	-3.0V		+V_{CC}
+V	9.0V	CLK	32 μSEC
-V	9.0V	REF CLK	+OSC

ROW ASSIGNMENT	
10	—
1	—
2	+V
3	-V
4	-V
5	ØV
6	+B4
7	—
8	—
9	—

INPUT PINS	COL	SIG
	63	-C0
	64	-C1
	65	-C2
	66	-C
	67	-C4
	68	+C5
	69	-C6
	70	+B0
	71	+B1
	72	+B2
	73	+B3
1, 2, 18	74	+B4
	75	+B5
	76	+B6
	77	+B7
	78	-S0
	79	+S1
	80	+S2
		+CO REF

OUTPUT PINS (TEST POINTS)	SWITCH SETTING
7, 3, 19 (2)	A/B: 1 2 | 2 1 | 3 11 | 4 10 | 5 9

WAVEFORMS — 128 μ SEC

DYNATRONICS TESTAGRAM

 + B0 REF

NOTES :

1. VCC (+5EXT) LOGIC SUPPLY ADJUSTED TO +4.75V.
2. THIS PROGRAM IS FOR POLAR INPUT OPERATION ONLY.

COVT APPD._____ DATE_____

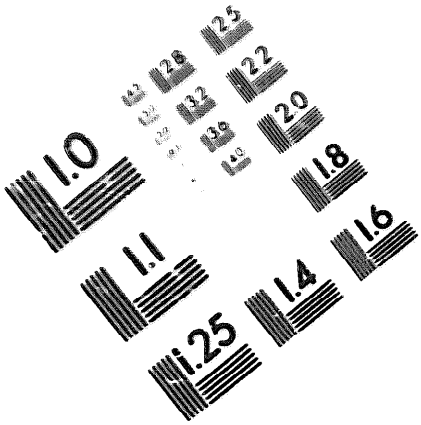
END

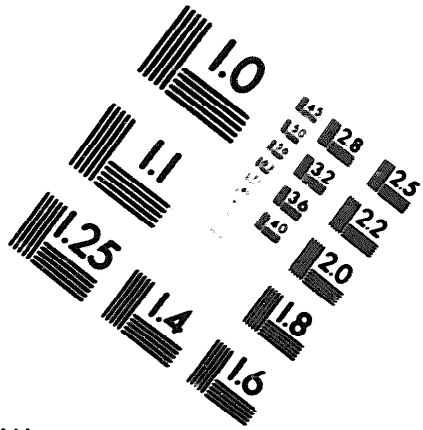
02-05-83

DATE

DEPARTMENT OF THE ARMY

MICROFORM
TEST TARGET





150 MM

1.5 mm (e= 1.0? mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1.37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

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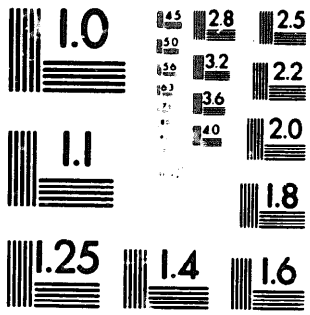

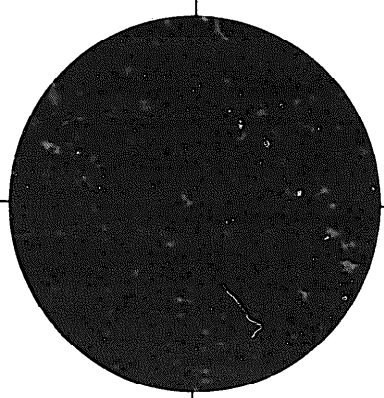

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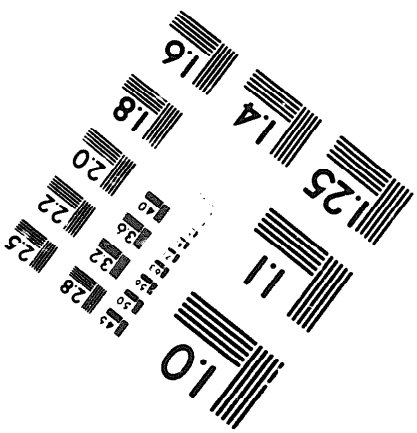

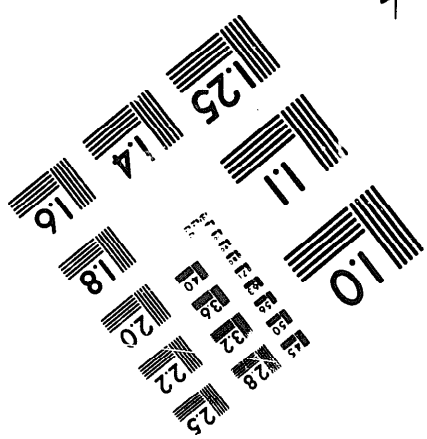

250 MM